

FIG. 1 (PRIOR ART)

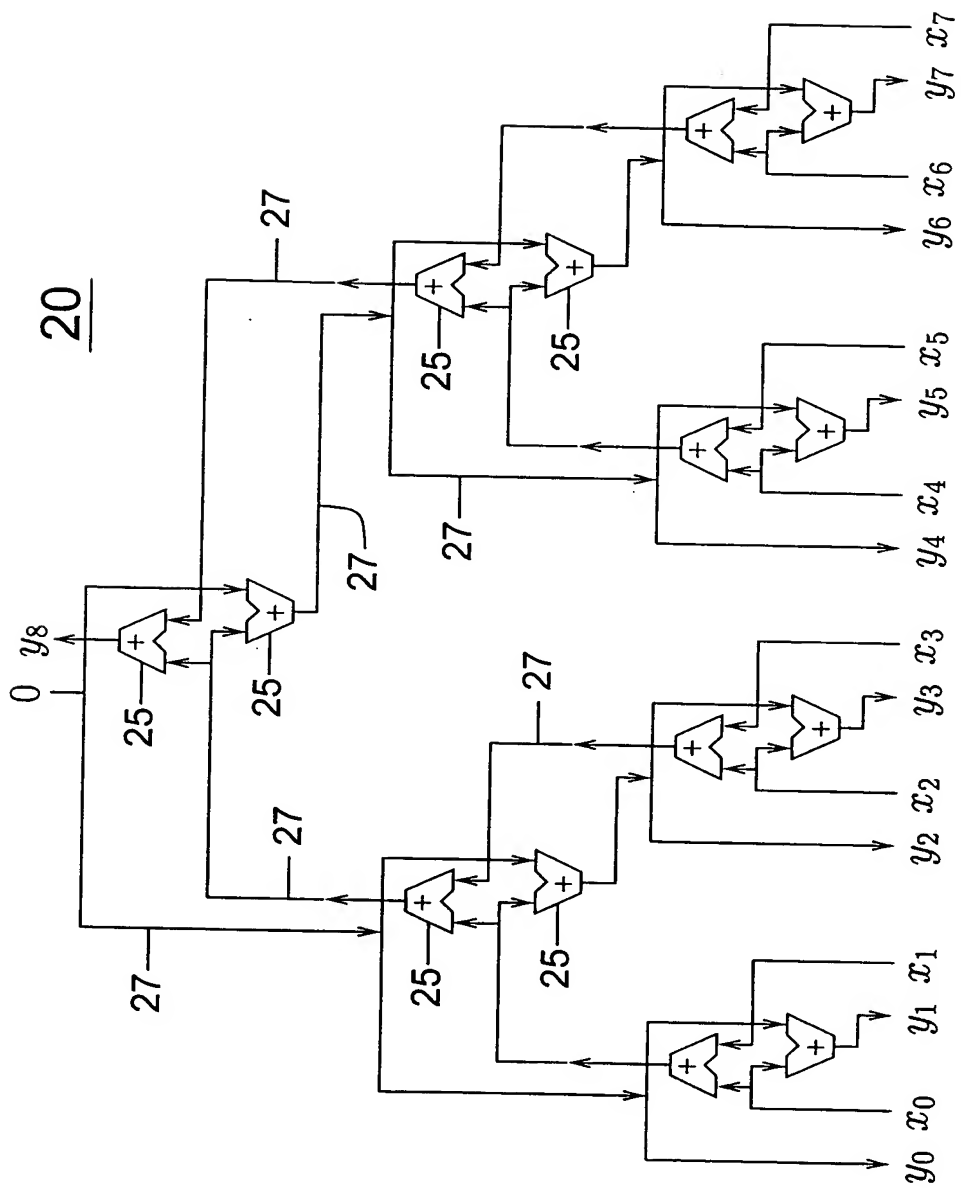


FIG. 2 (PRIOR ART)

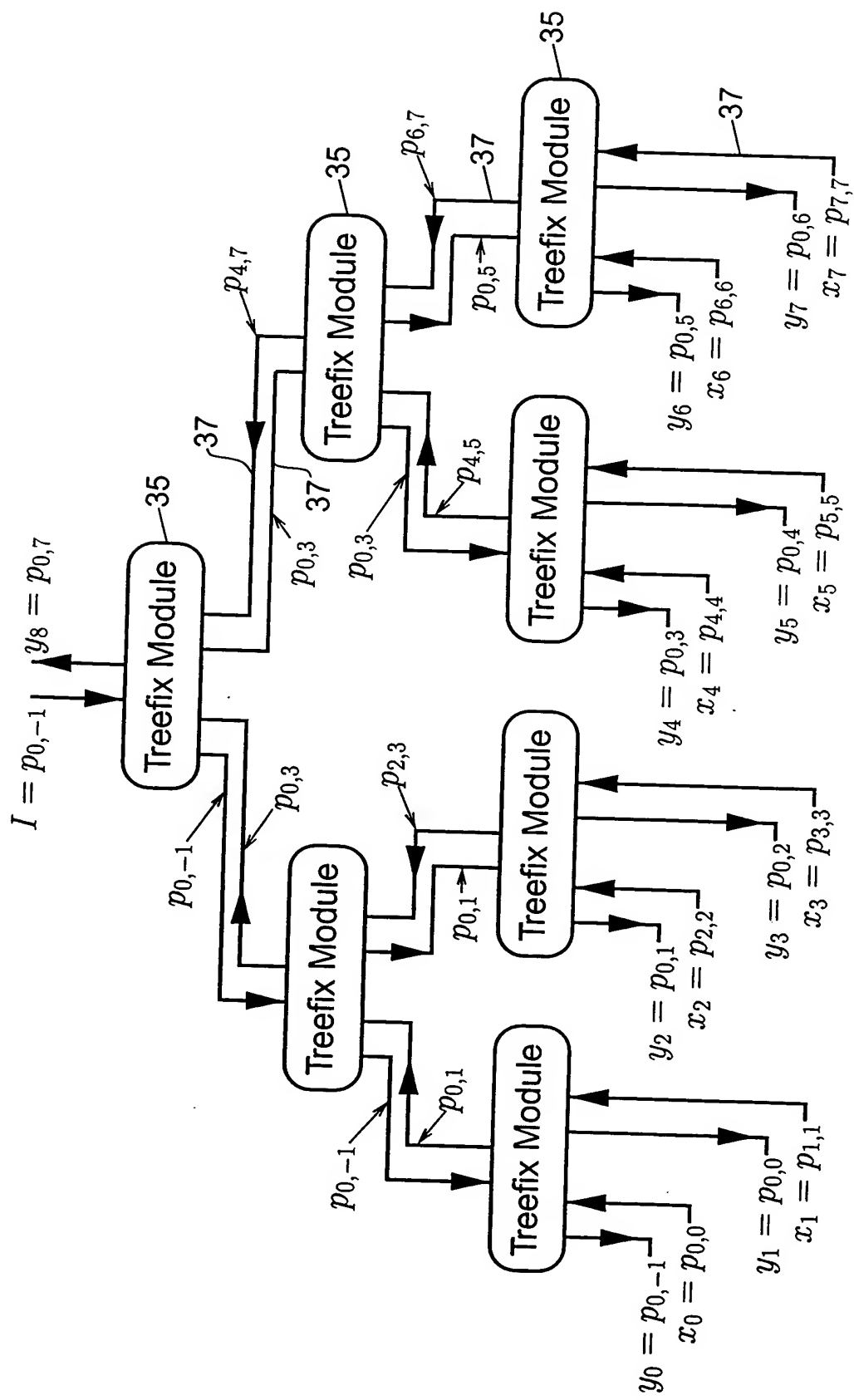
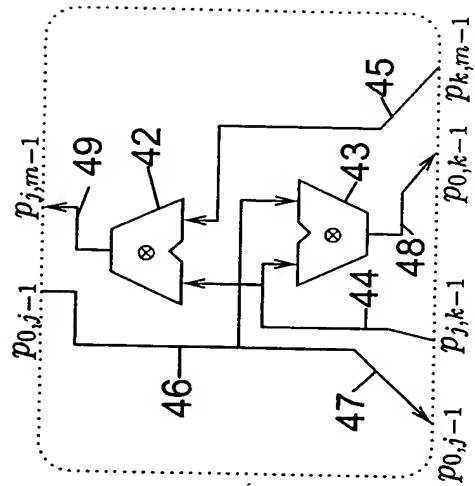


FIG. 3 (PRIOR ART)



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FIG. 4 (PRIOR ART)

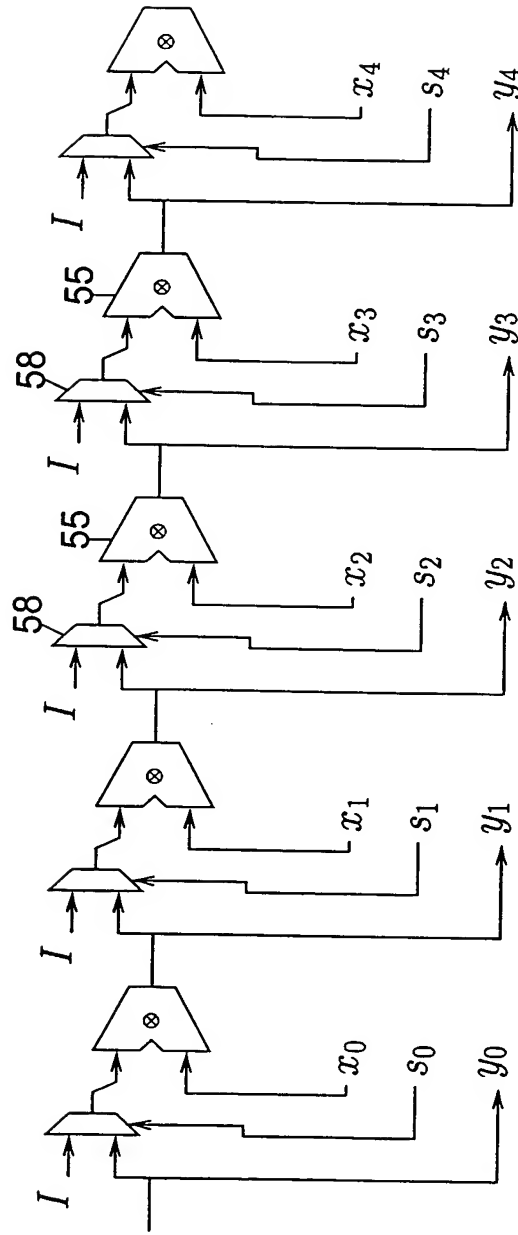


FIG. 5 (PRIOR ART)

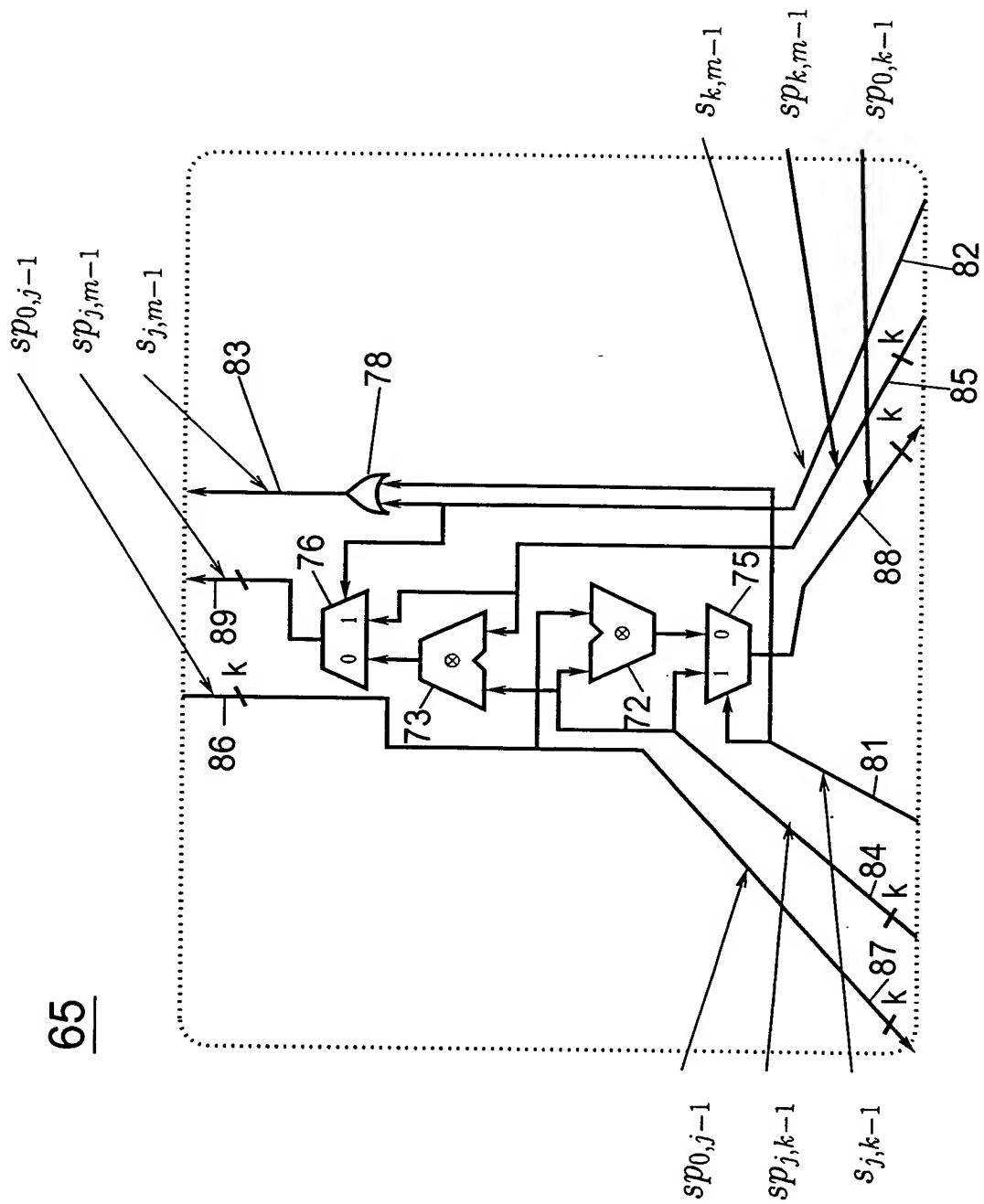


FIG. 7 (PRIOR ART)

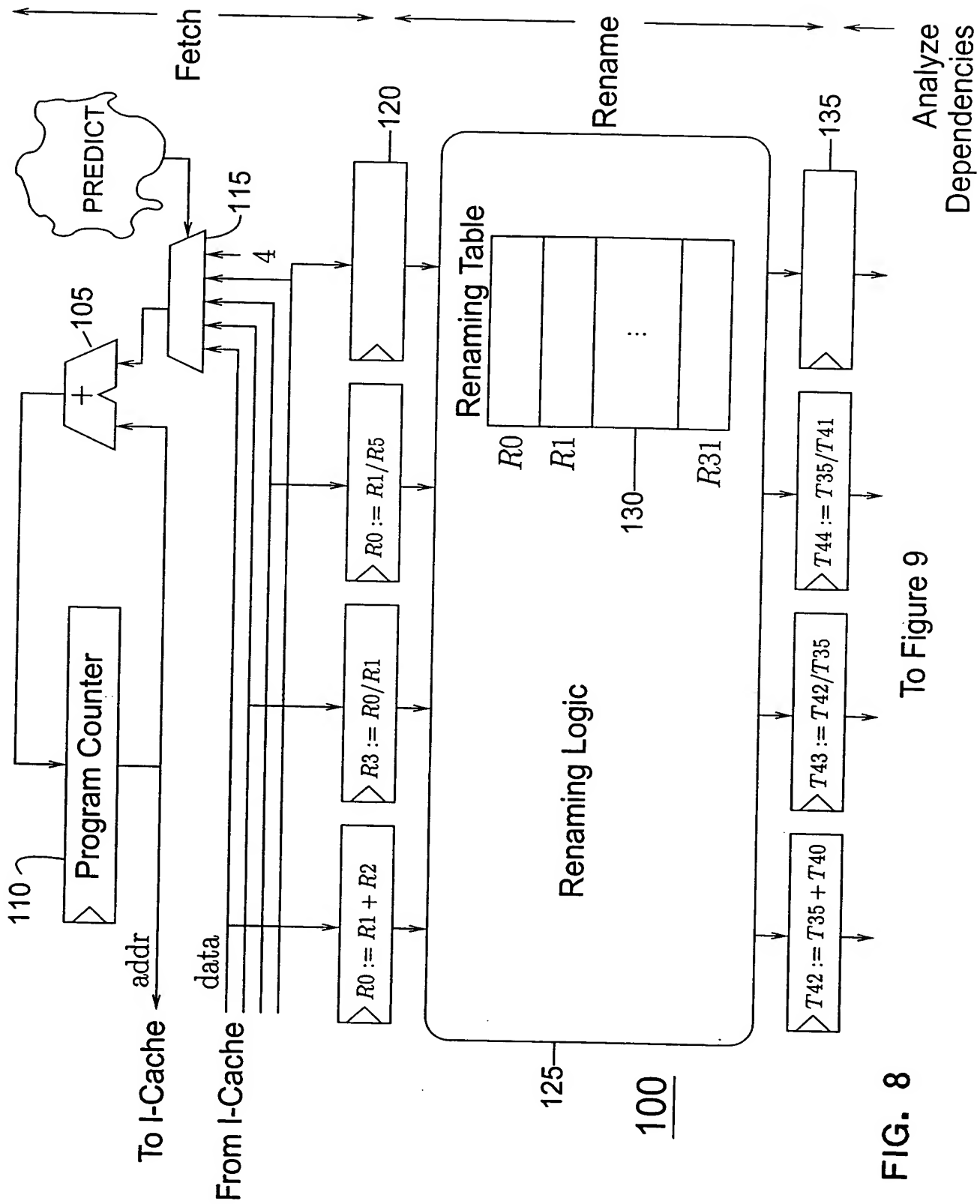


FIG. 8

To Figure 9

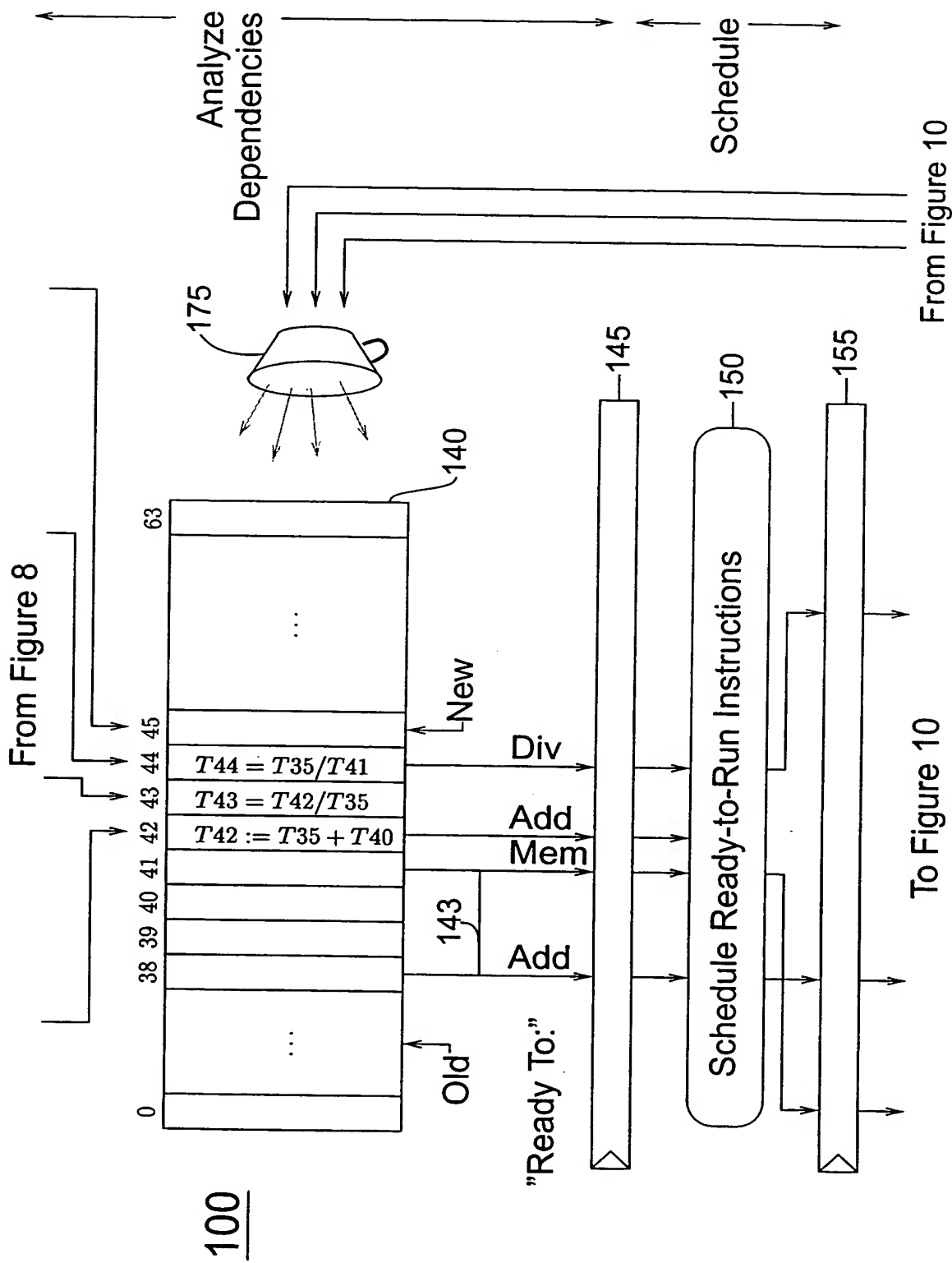


FIG. 9 (PRIOR ART)

100

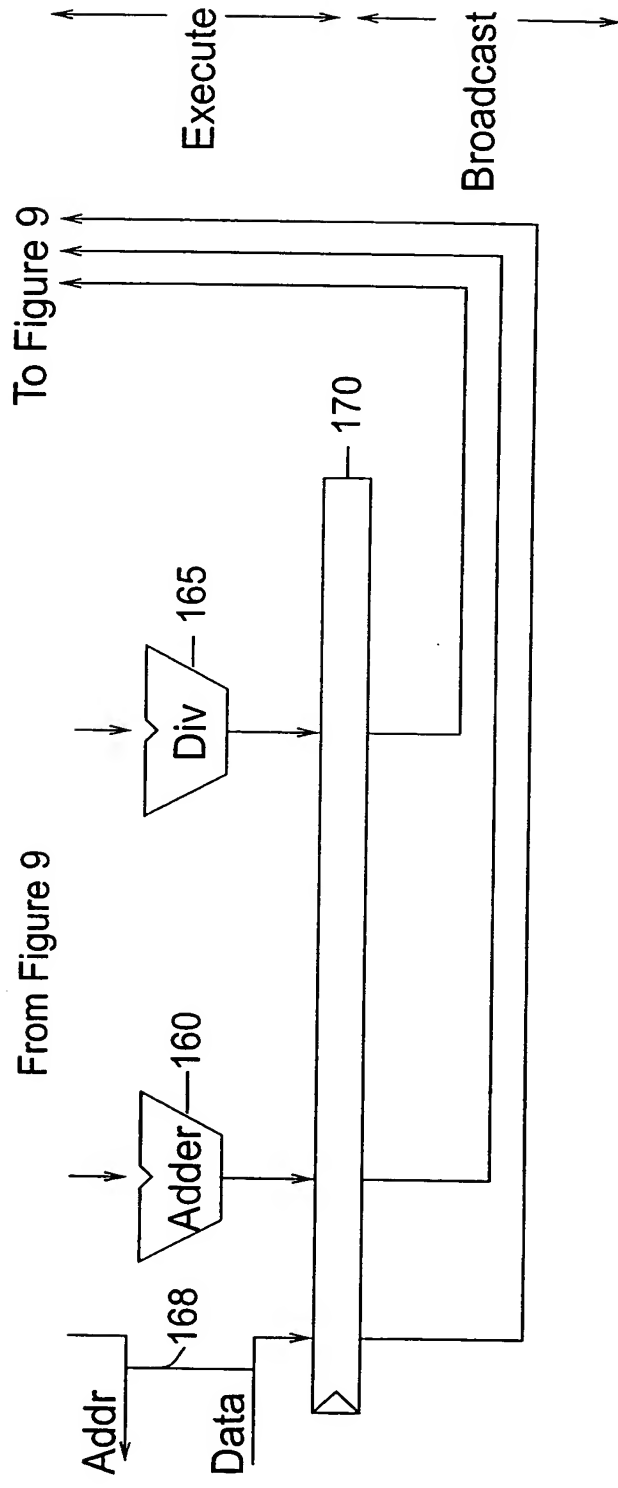


FIG. 10 (PRIOR ART)

Register	Tag	Register	Tag	Register	Tag	Register	Tag
0	30	0	42	0	42	0	44
1	35	1	35	1	35	1	35
2	40	2	40	2	40	2	40
3	25	3	25	3	43	3	43
4	26	4	26	4	26	4	26
5	41	5	41	5	41	5	41
Before		After Instruction 0		After Instruction 1		After Instruction 2	

FIG. 11

200

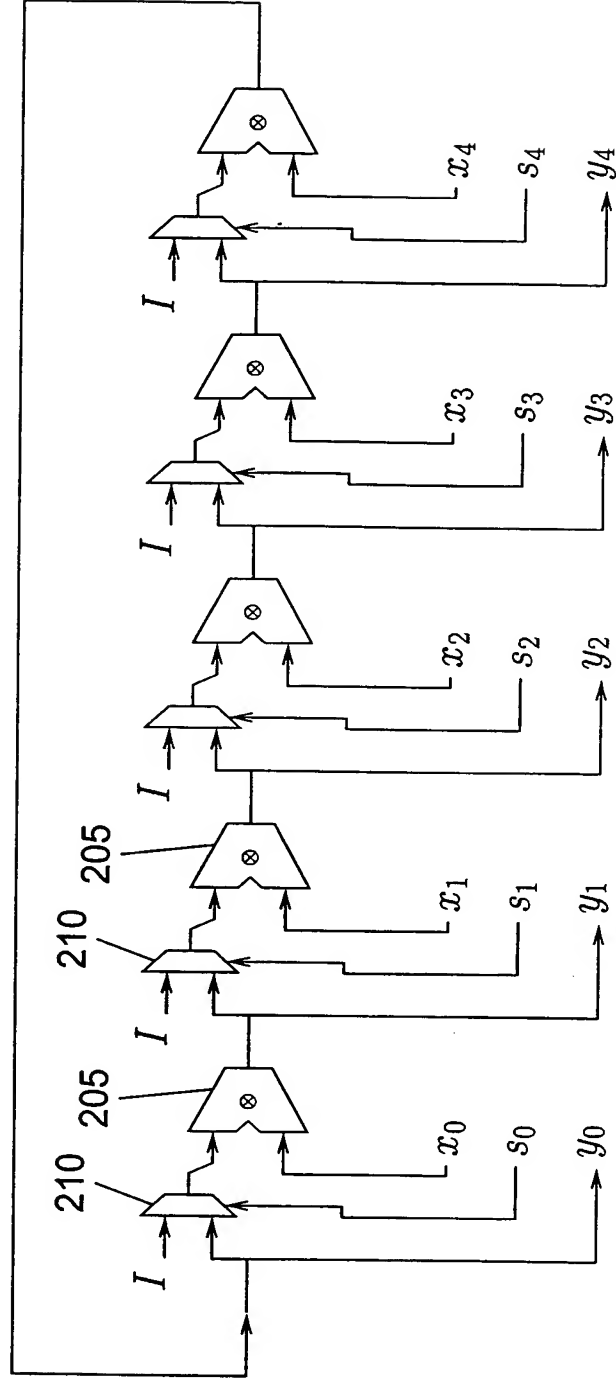


FIG. 12

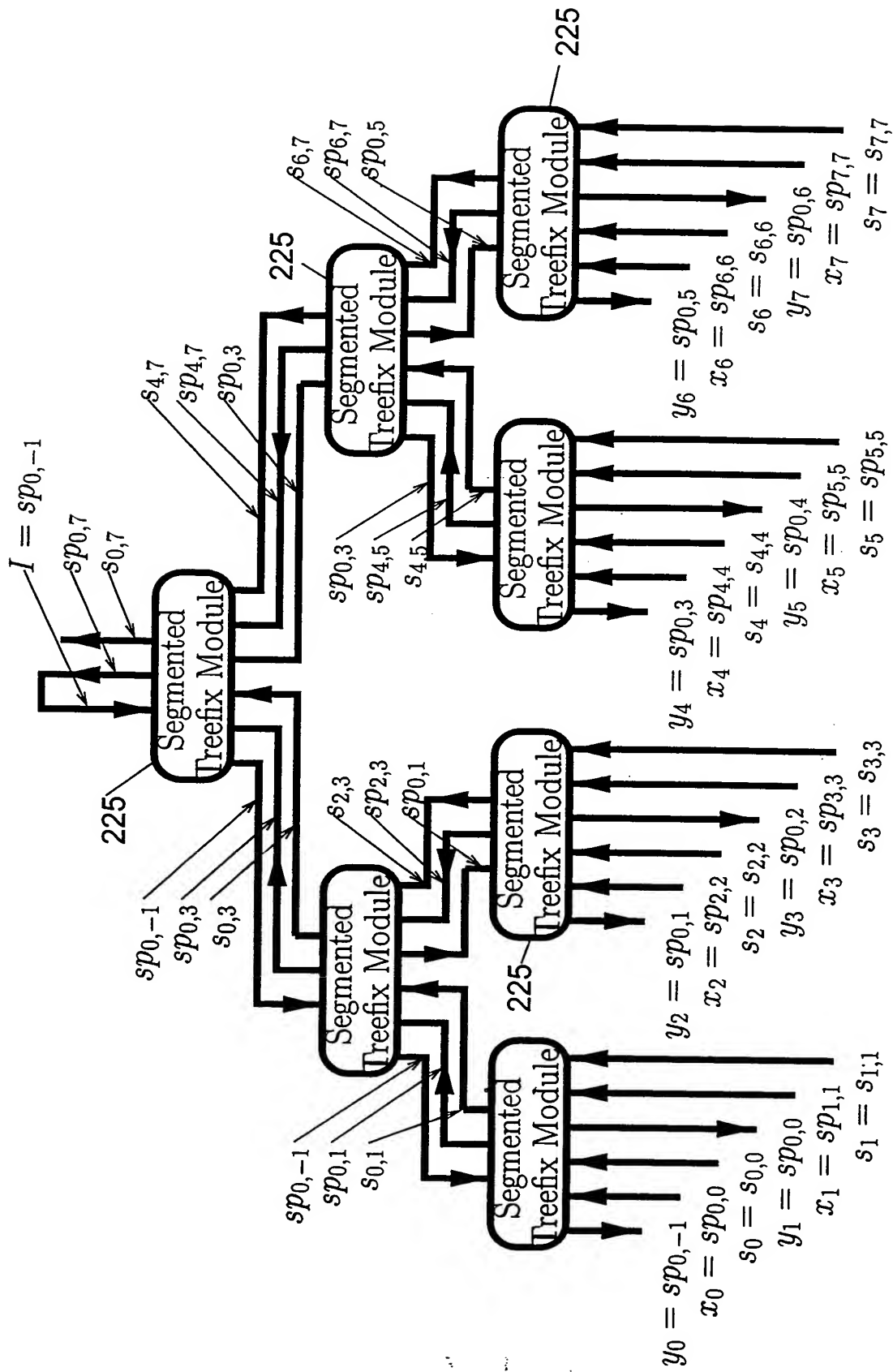


FIG. 13

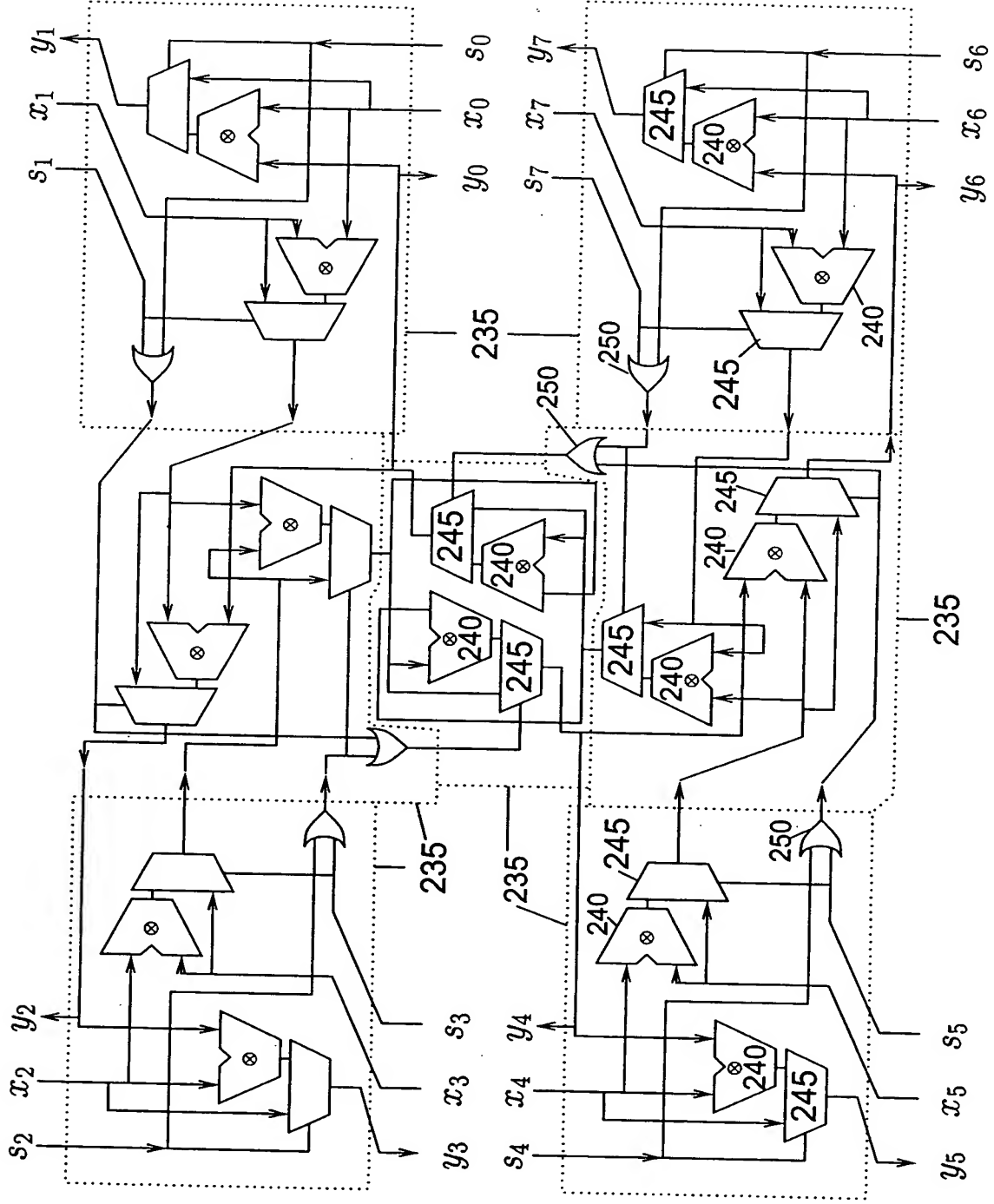


FIG. 14

260

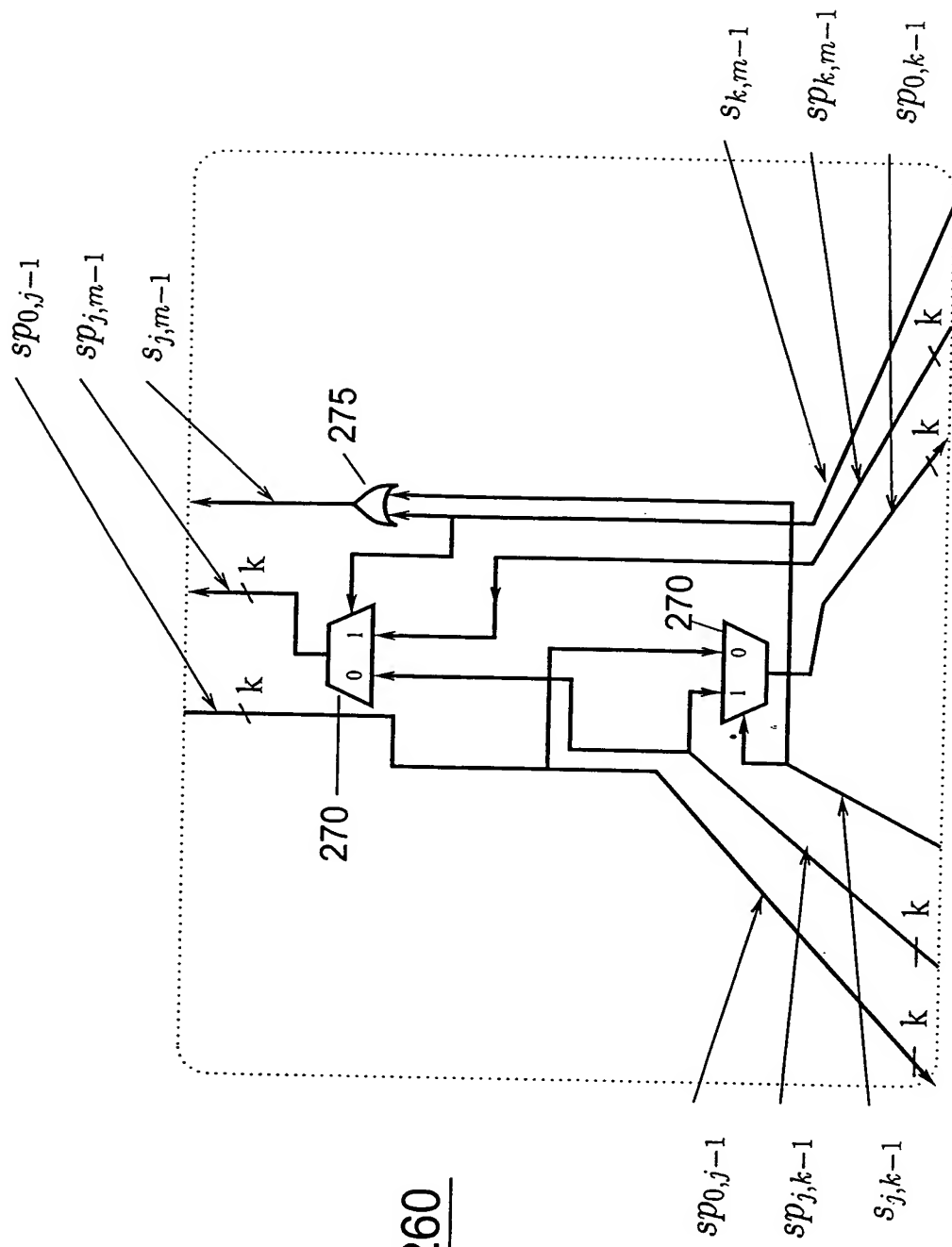


FIG. 15

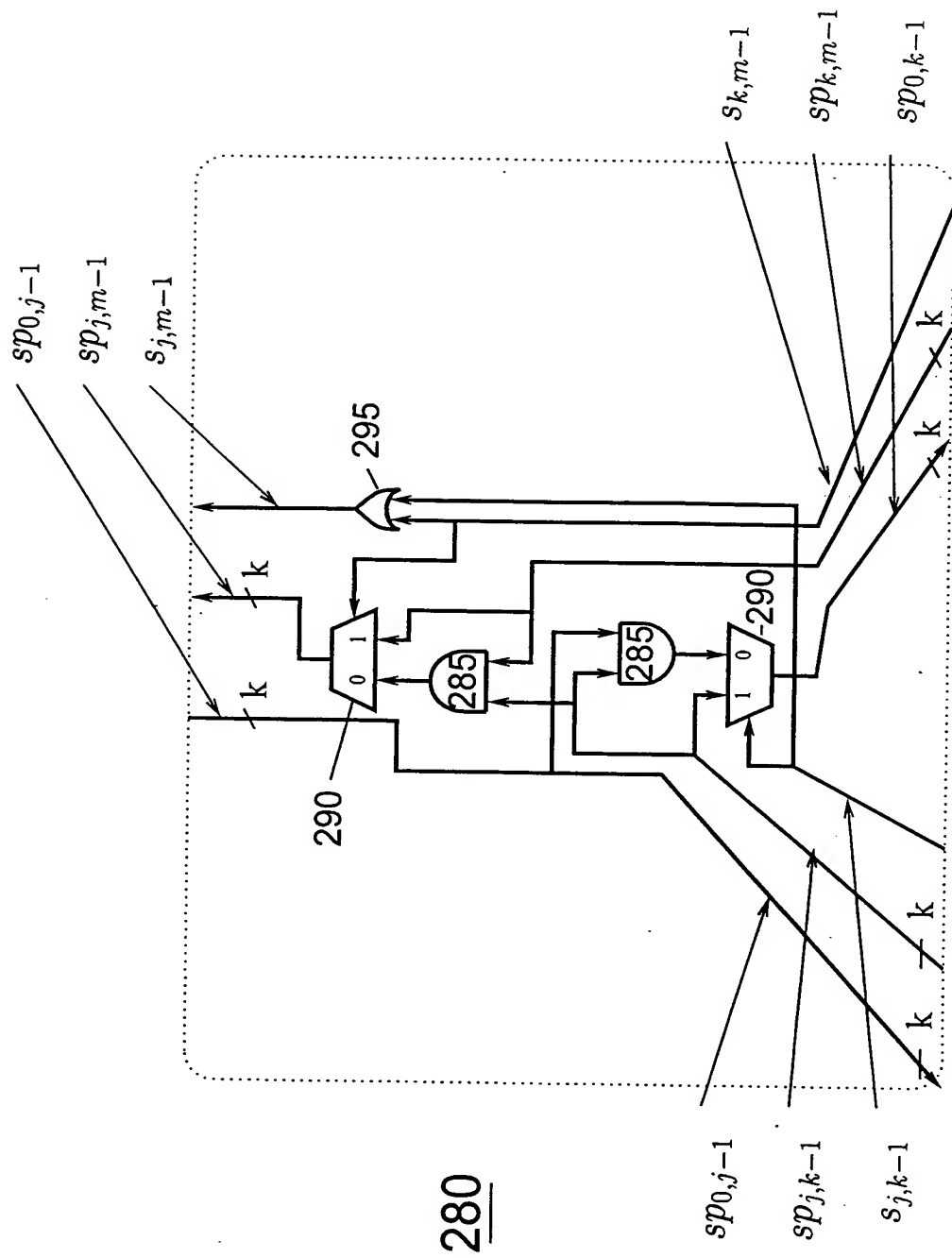


FIG. 16

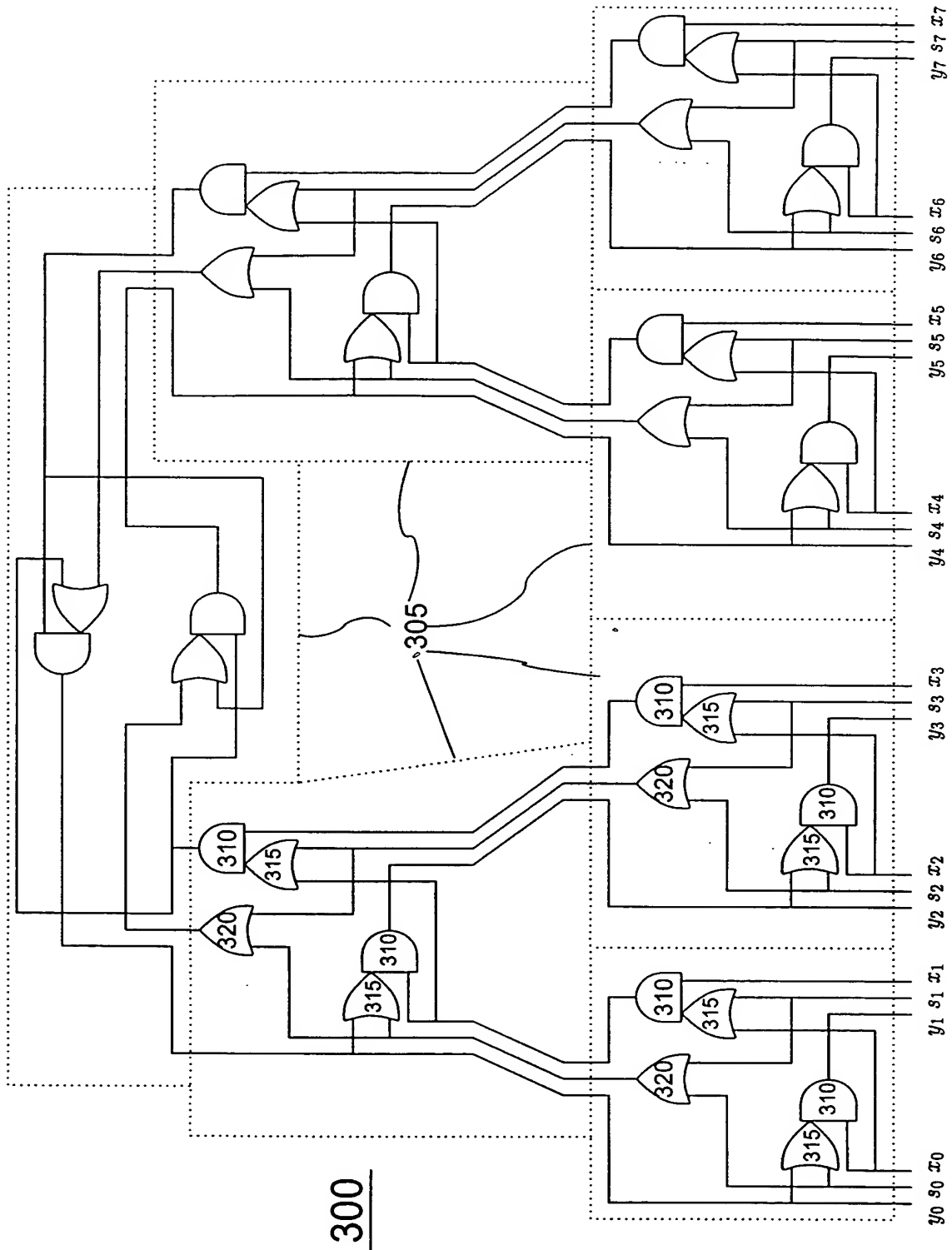


FIG. 17

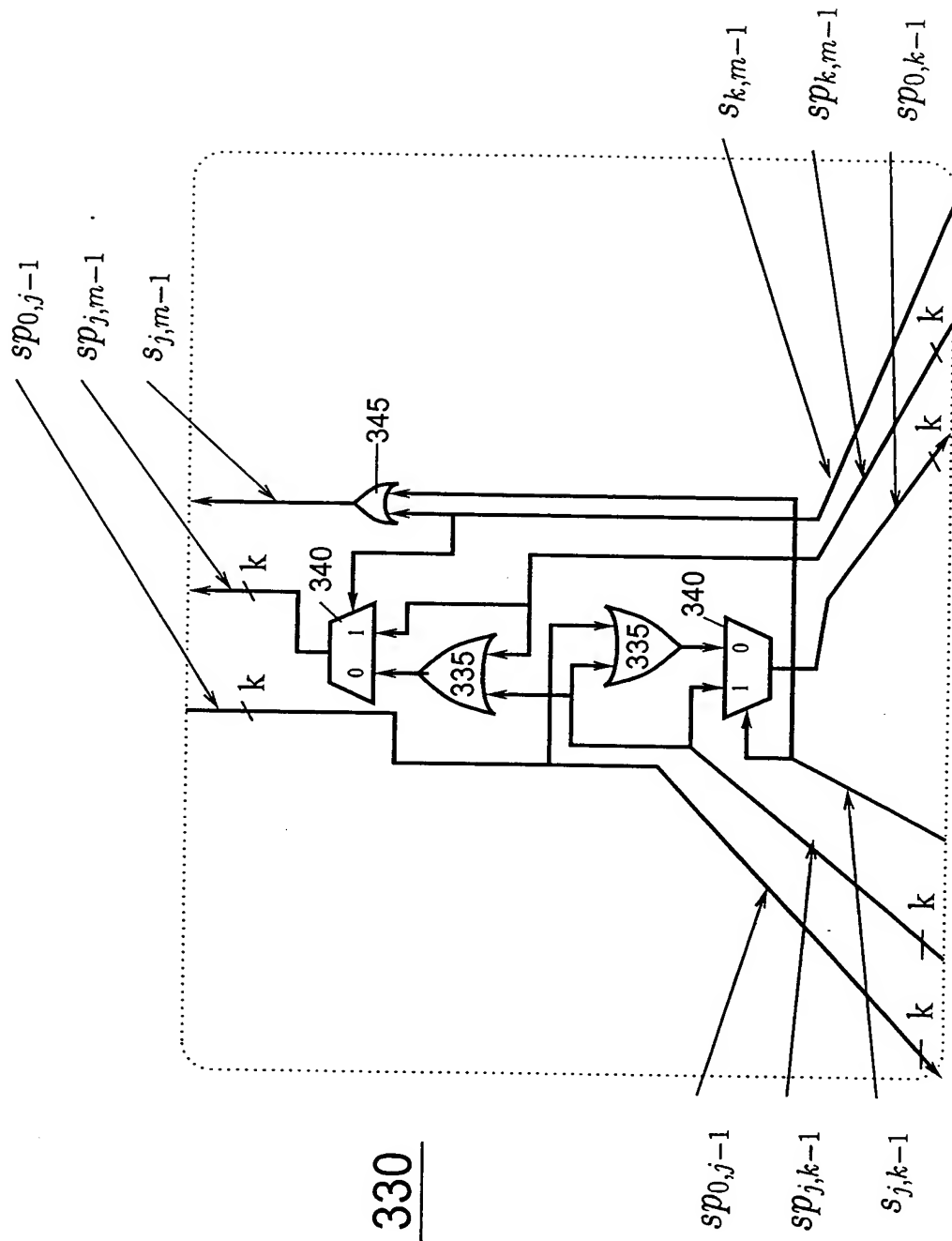


FIG. 18

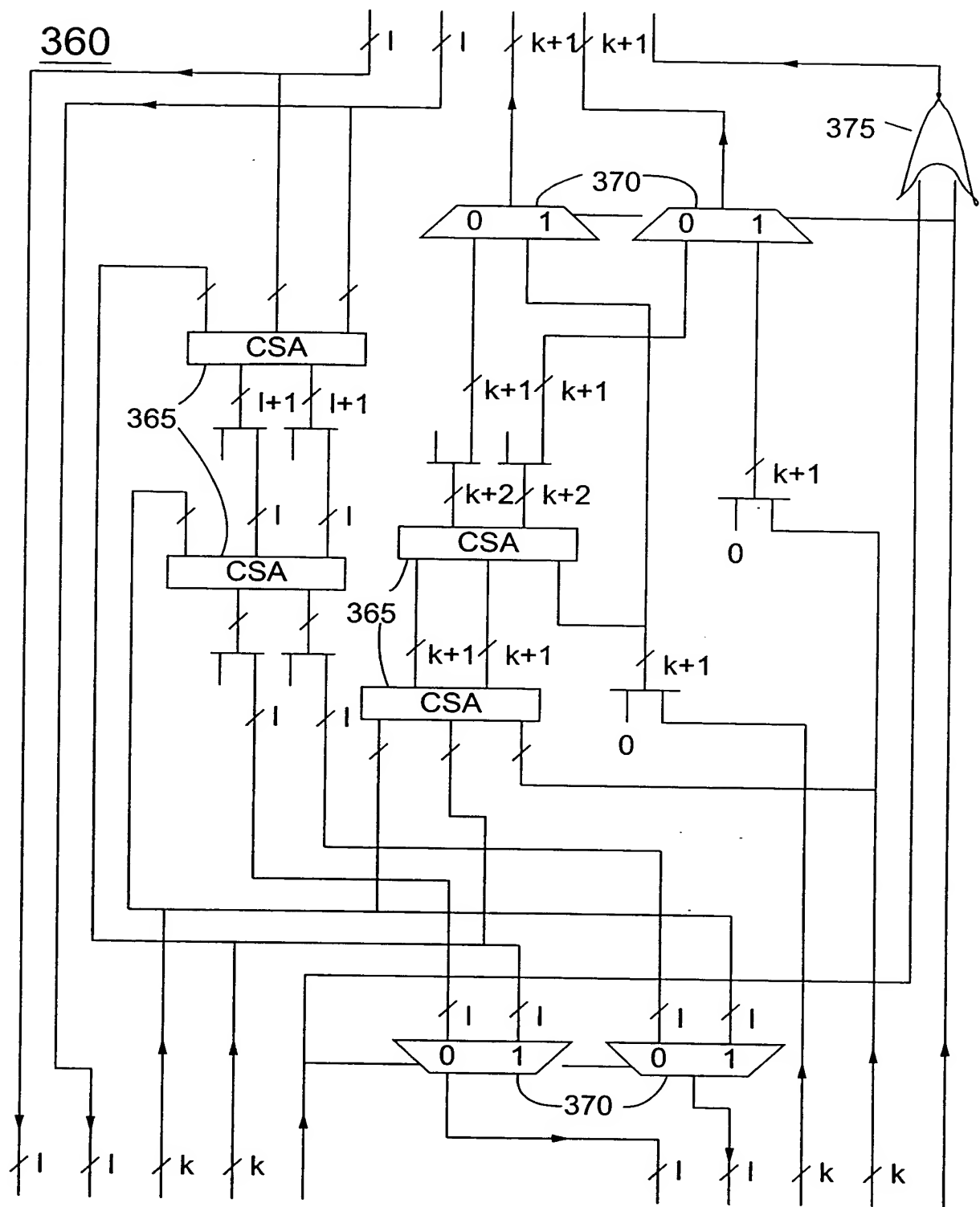


FIG. 19

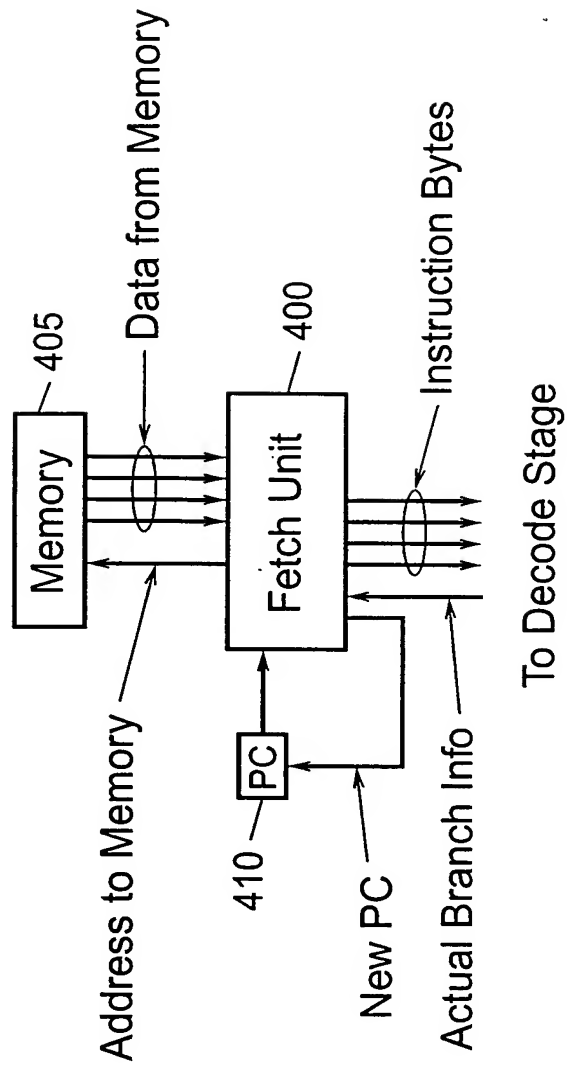


FIG. 20 (PRIOR ART)

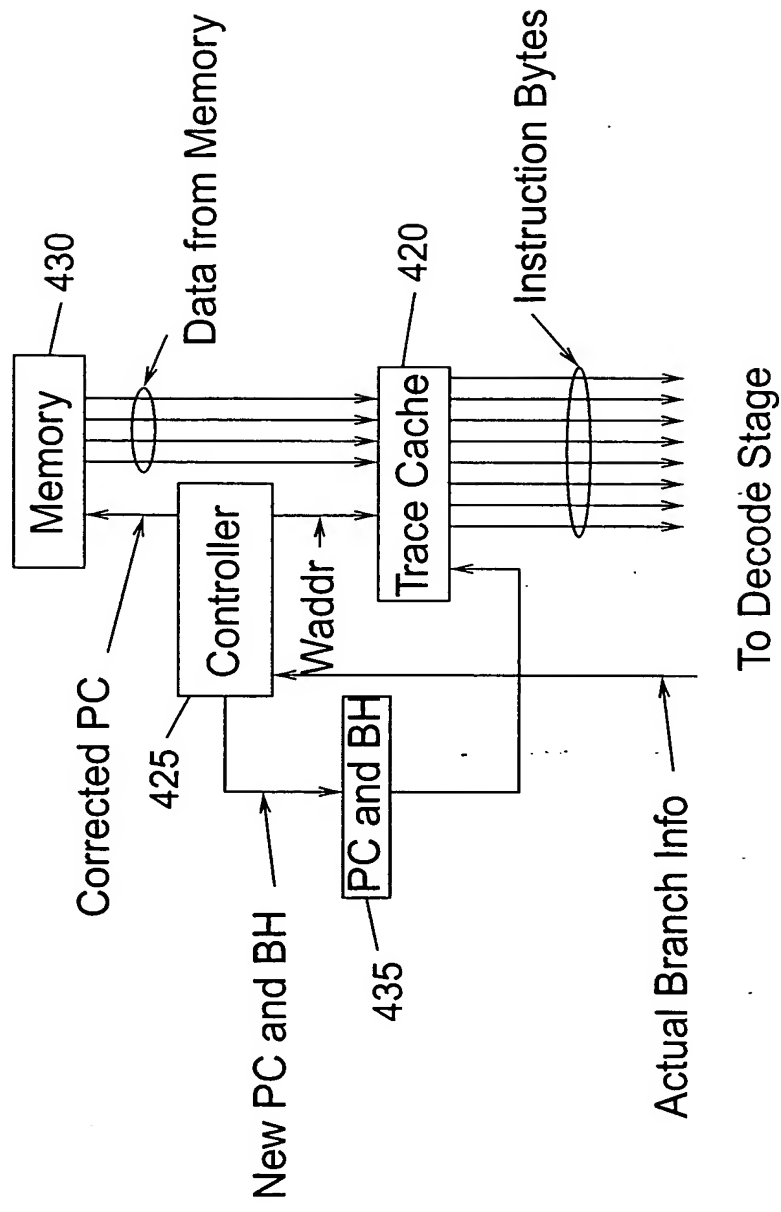
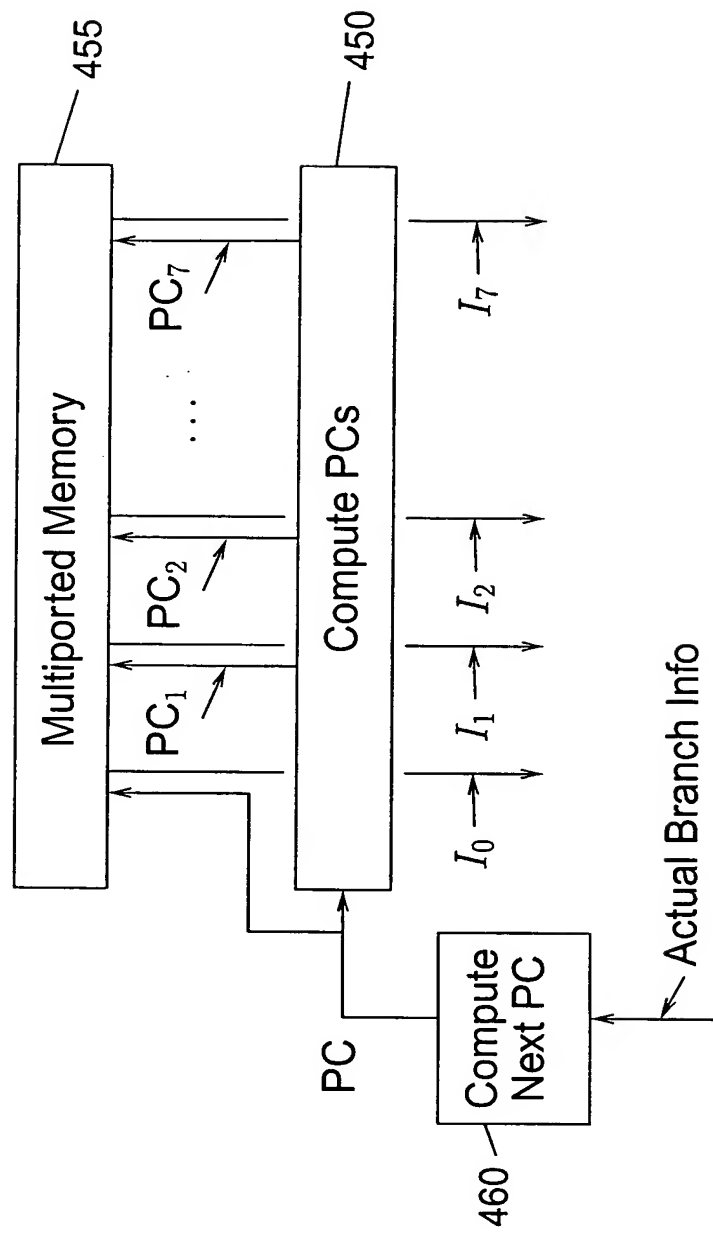
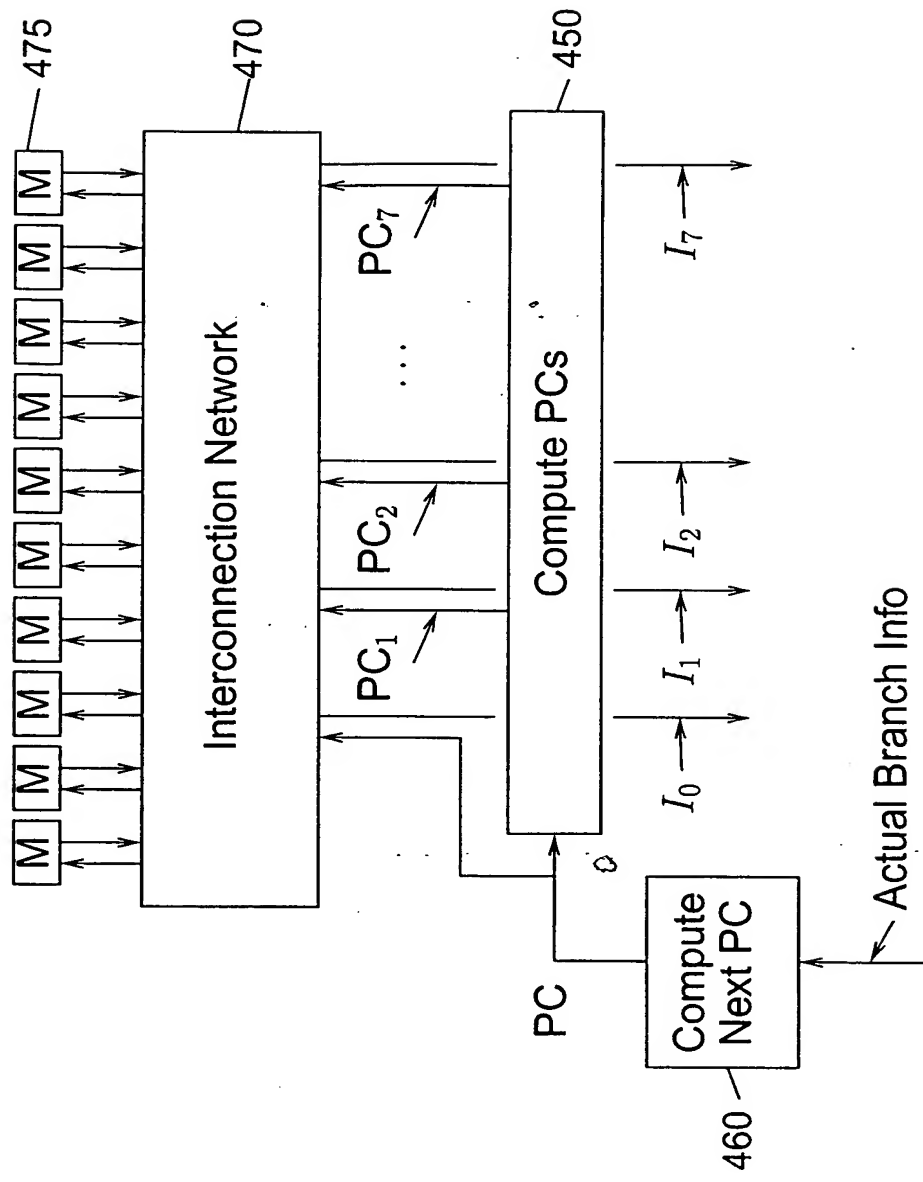


FIG. 21 (PRIOR ART)



To Decode Stage

FIG. 22



To Decode Stage

FIG. 23

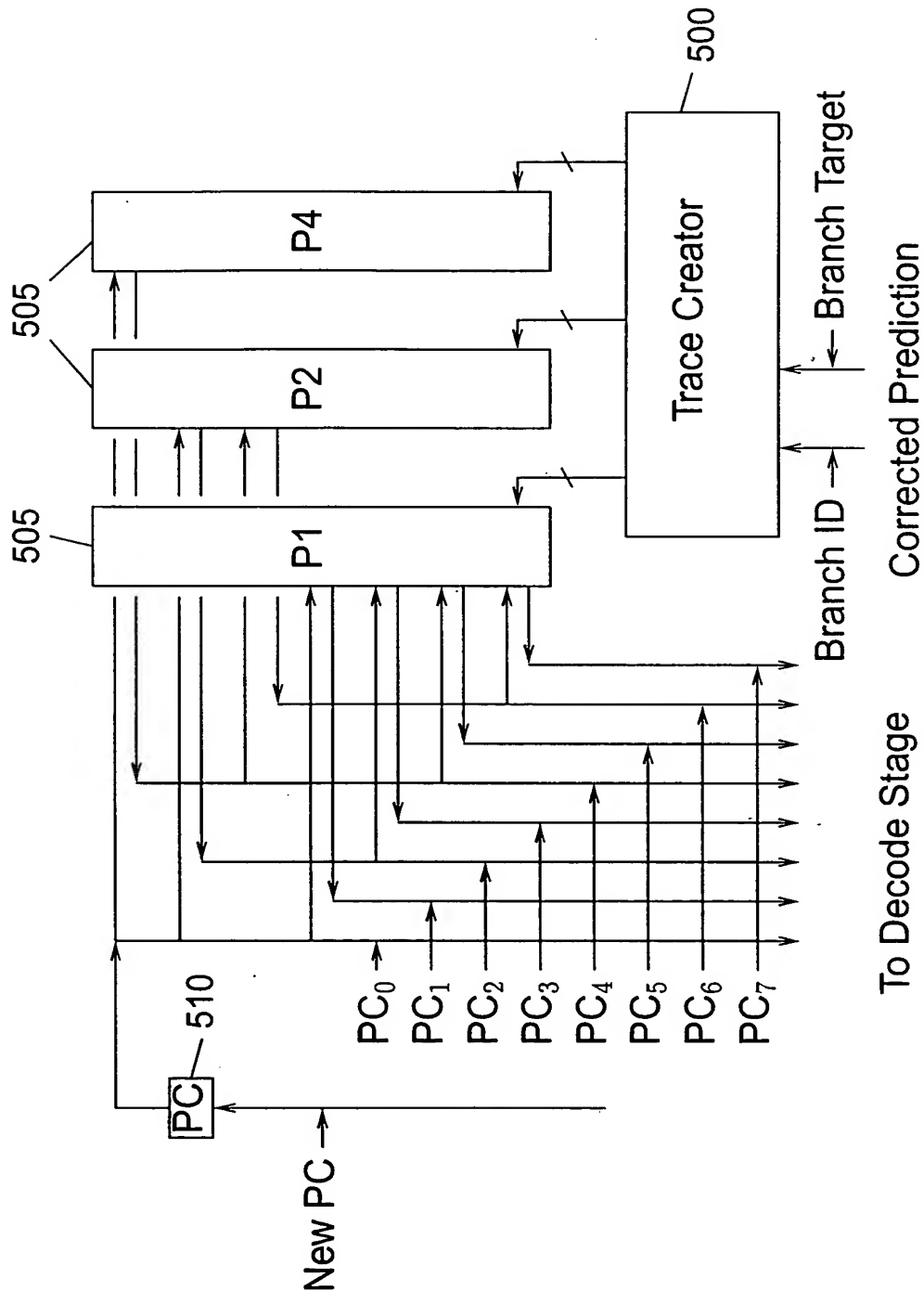
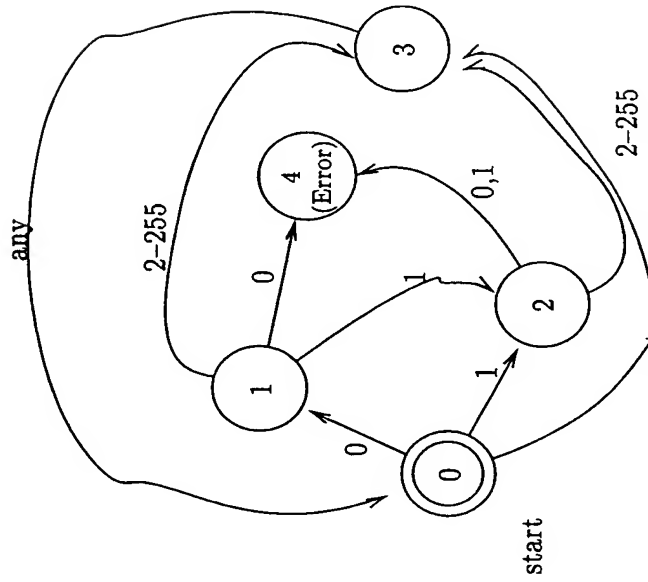


FIG. 24



(a) State transition diagram.

State	input				
	0	1	2	3	4
0	1	4	2	3	3
1	4	4	4	3	3
2	3	0	0	0	0
3	4	4	4	4	4

(b) State transition table.

FIG. 25

Input	0	1	3	0	1	3	0	1
Level 0	1	2	3	1	2	3	1	2
	4	2	3	4	2	3	4	2
	4	4	3	4	4	3	4	4
	0	0	0	0	0	0	0	0
	4	4	4	4	4	4	4	4
Level 1	2		0		3		2	
	4		0		3		4	
	4		0		4		4	
	2		0		3		2	
	4		0		4		4	
Level 2	0				2			
	4				2			
	4				4			
	0				2			
	4				4			
Level 3					2			
					4			
					4			
					2			
					4			

FIG. 26

$$(x \otimes y) = \begin{bmatrix} (x \otimes y)_0 \\ (x \otimes y)_1 \\ (x \otimes y)_2 \\ (x \otimes y)_3 \\ (x \otimes y)_4 \end{bmatrix} = \begin{bmatrix} y_{x_0} \\ y_{x_1} \\ y_{x_2} \\ y_{x_3} \\ y_{x_4} \end{bmatrix} = \begin{bmatrix} y_1 \\ y_4 \\ y_4 \\ y_0 \\ y_4 \end{bmatrix} = \begin{bmatrix} 2 \\ 4 \\ 4 \\ 2 \\ 4 \end{bmatrix}$$

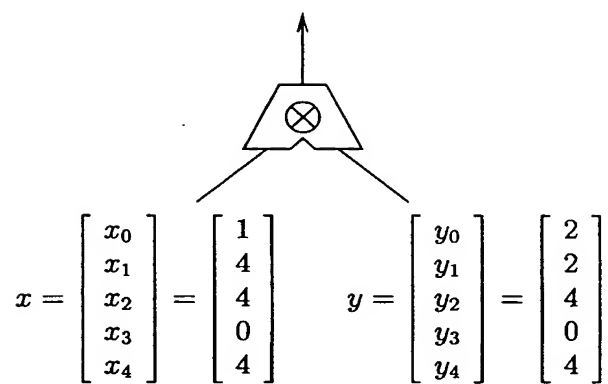


FIG. 27

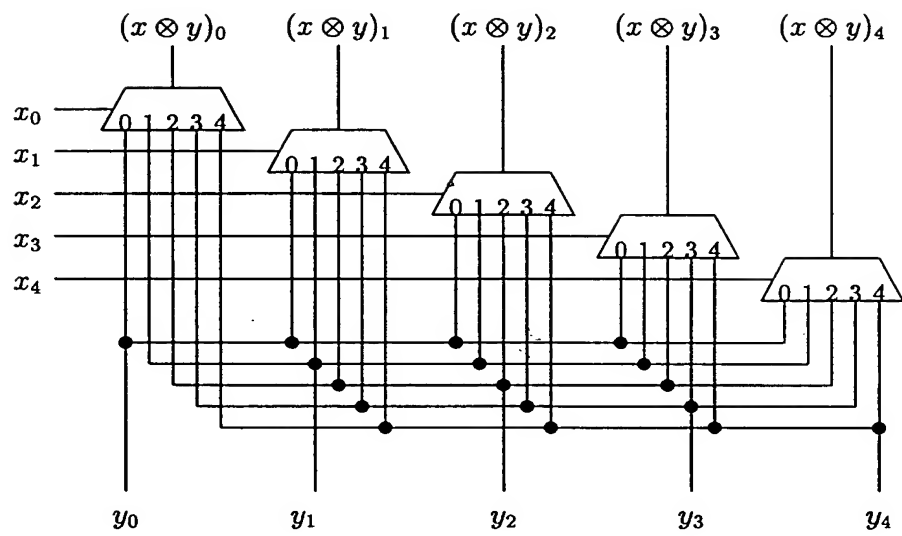
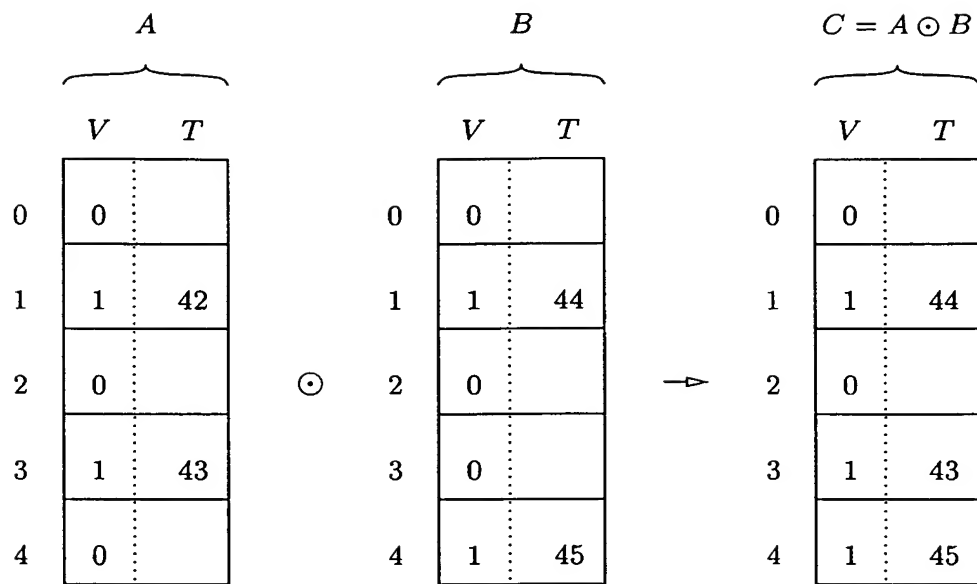


FIG. 28



Logic for one row:

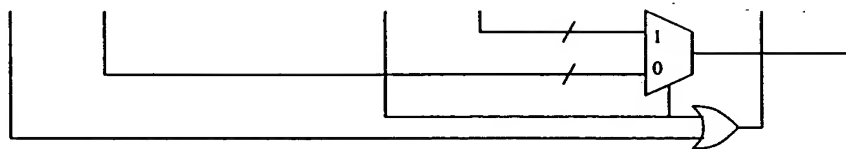


FIG. 29

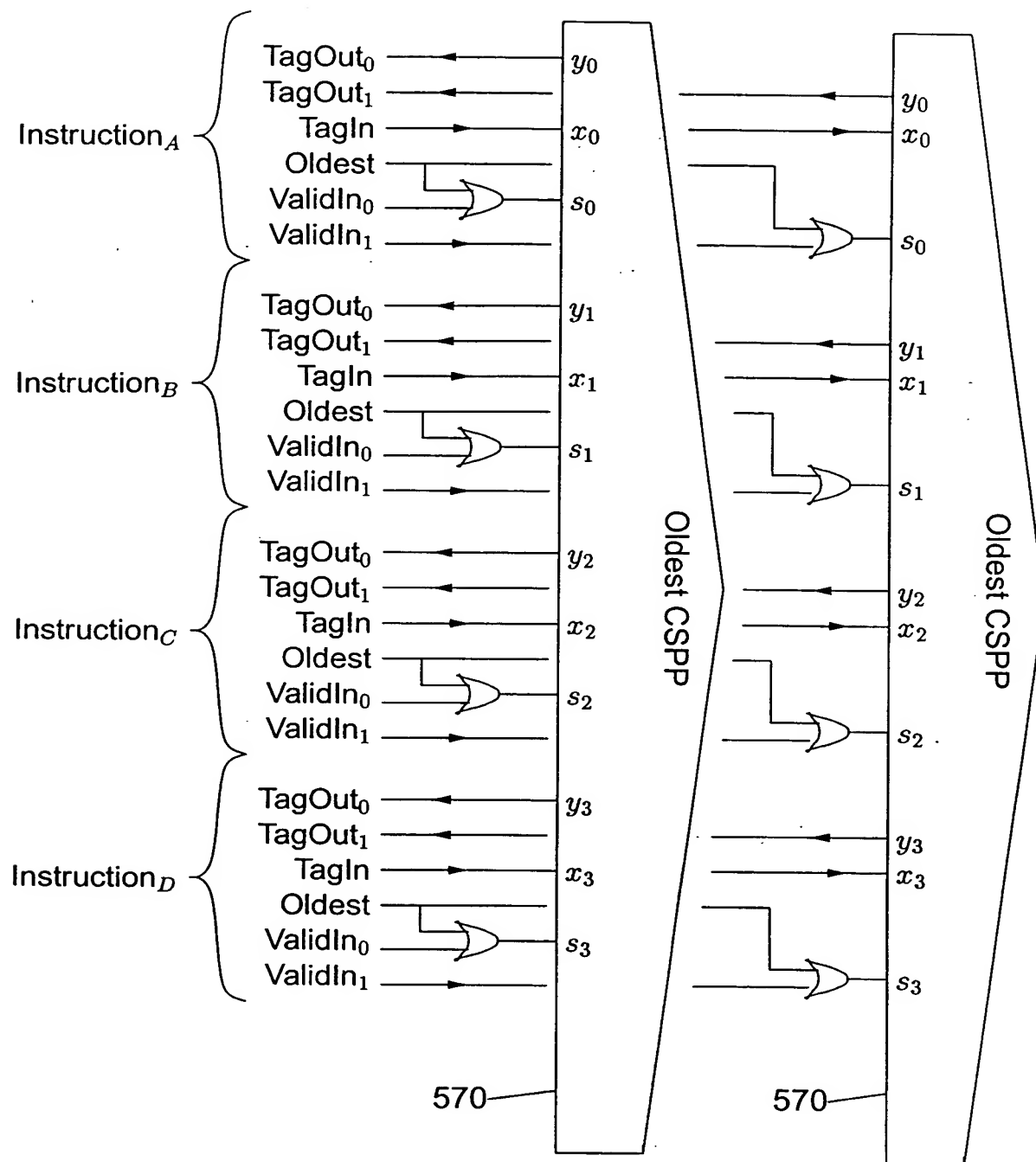


FIG. 30

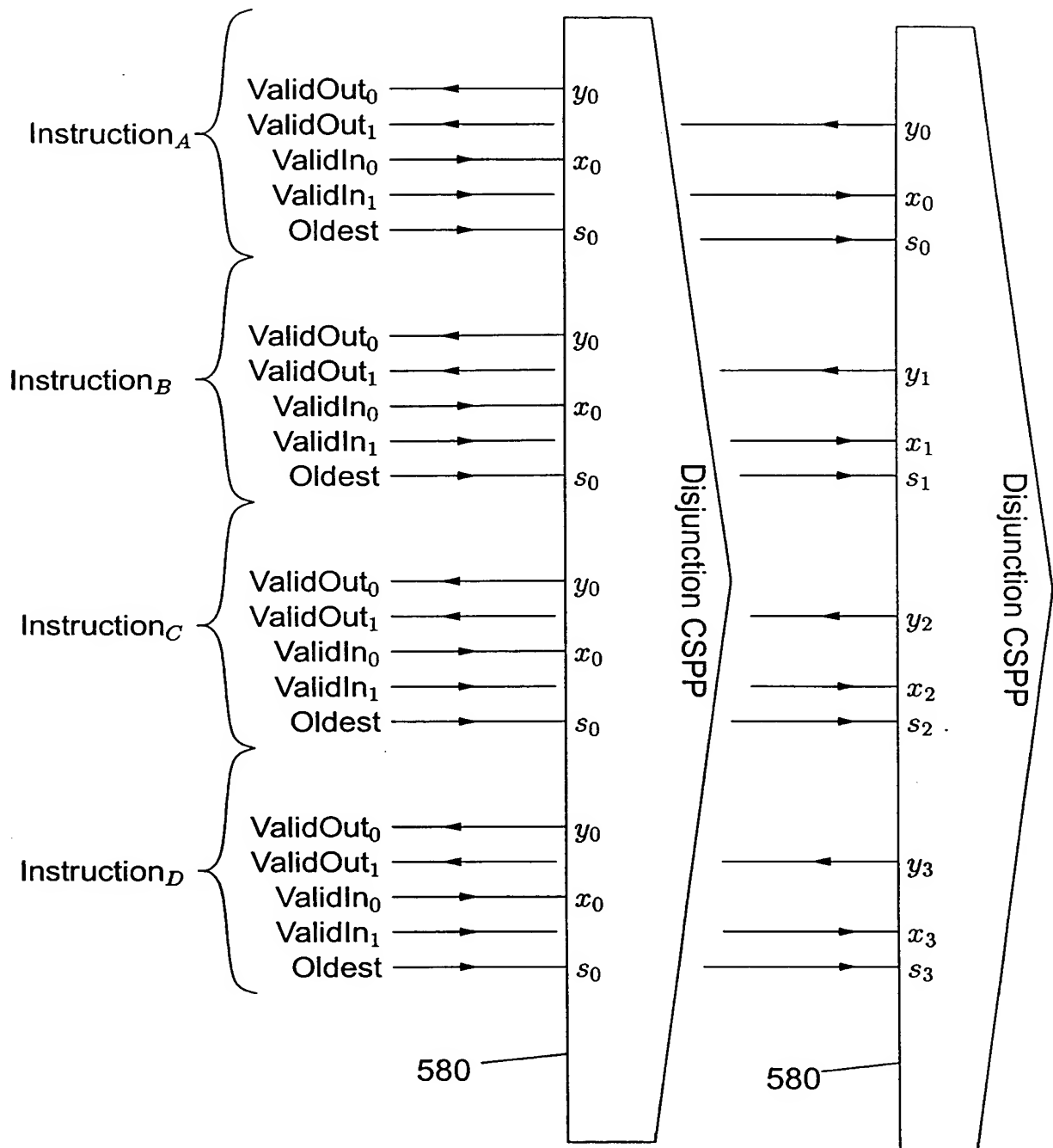


FIG. 31

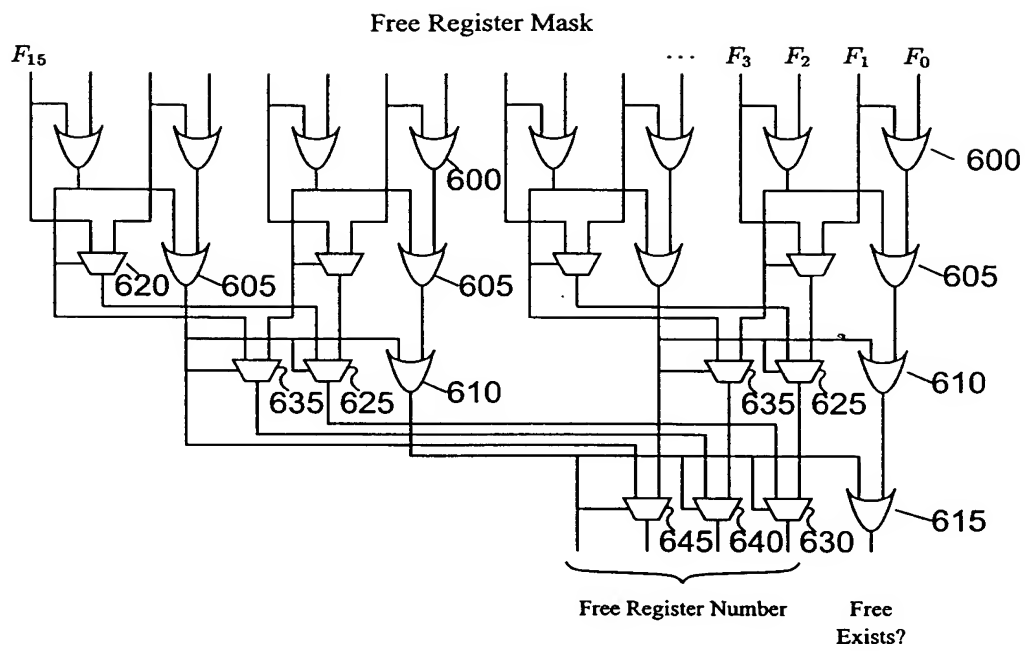


FIG. 32

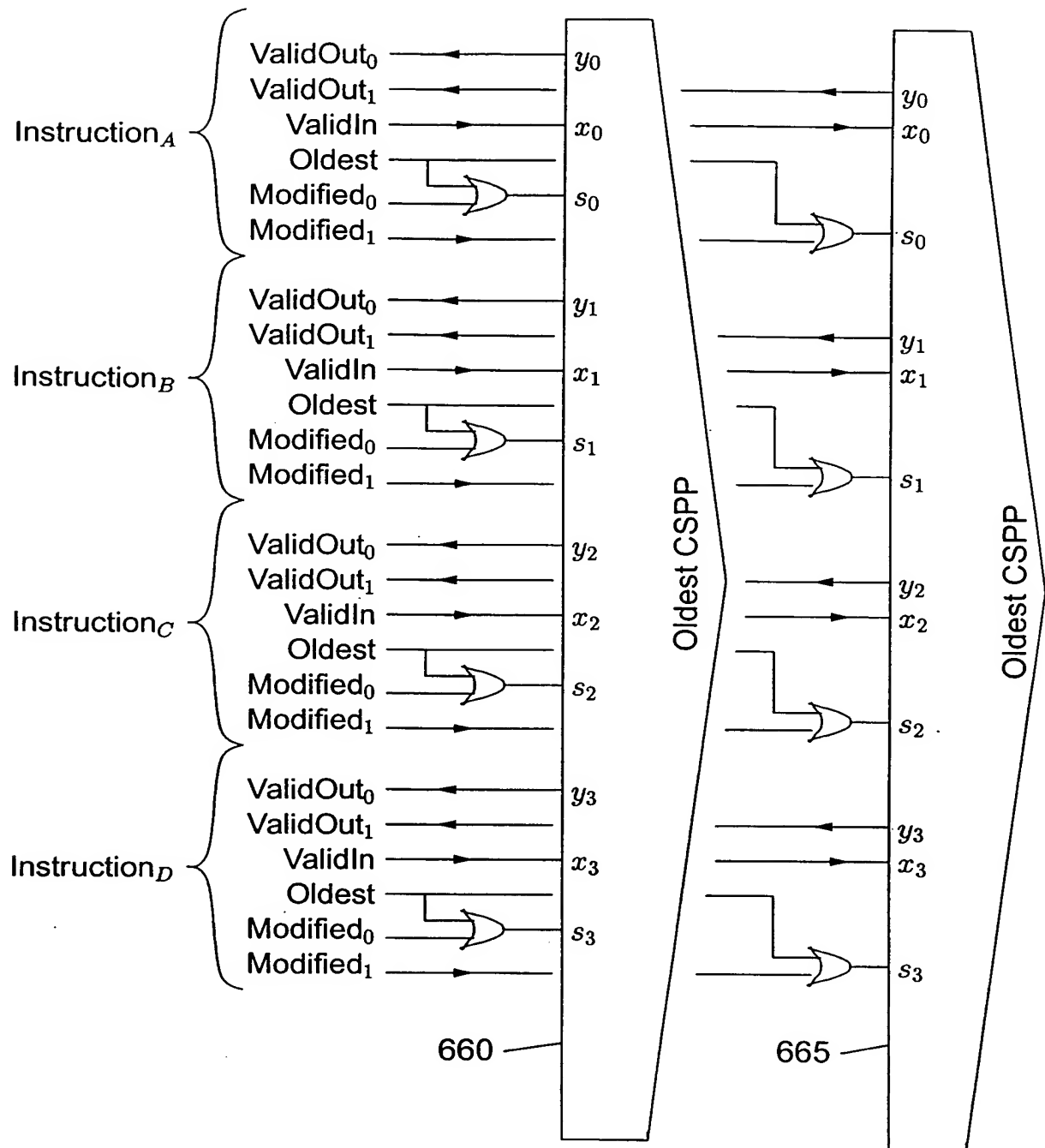


FIG. 33

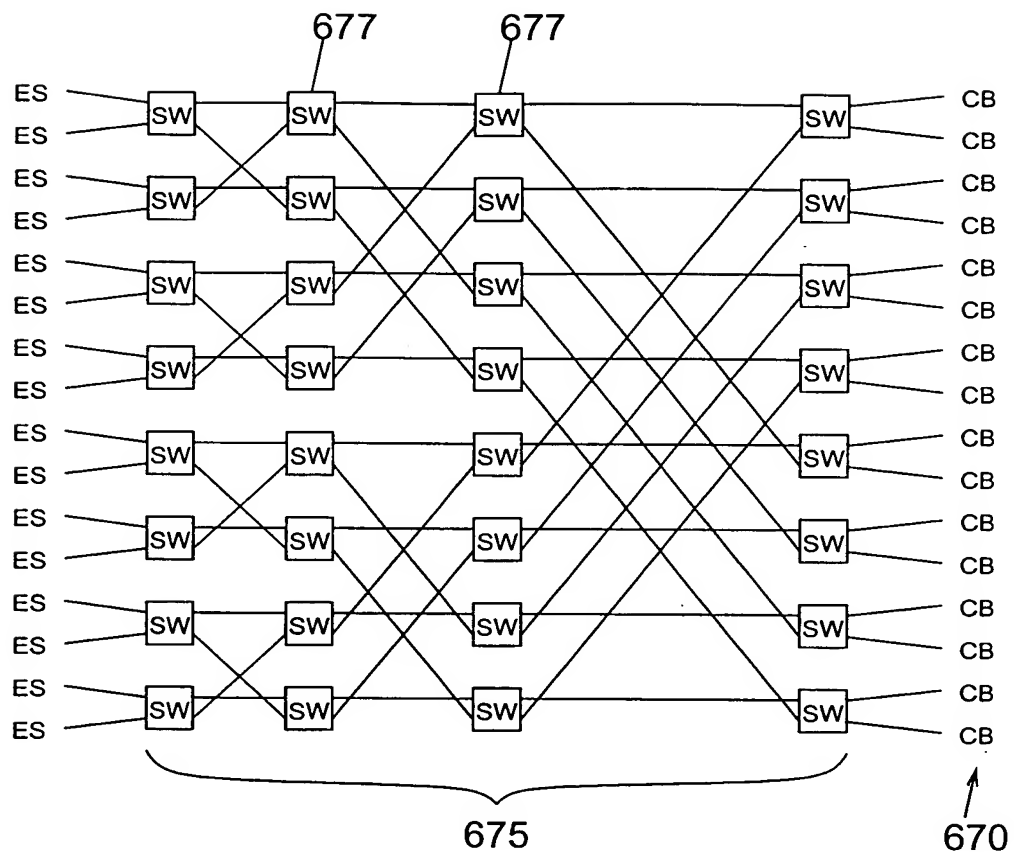


FIG. 34

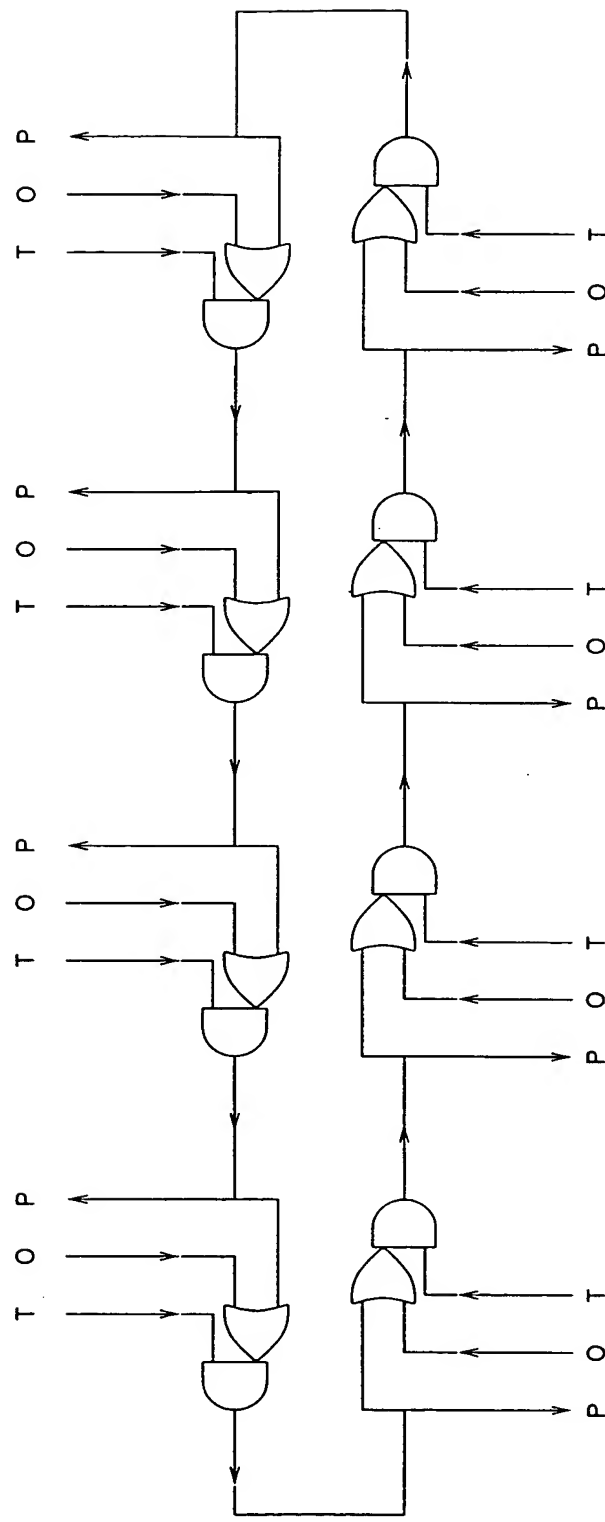


FIG. 35

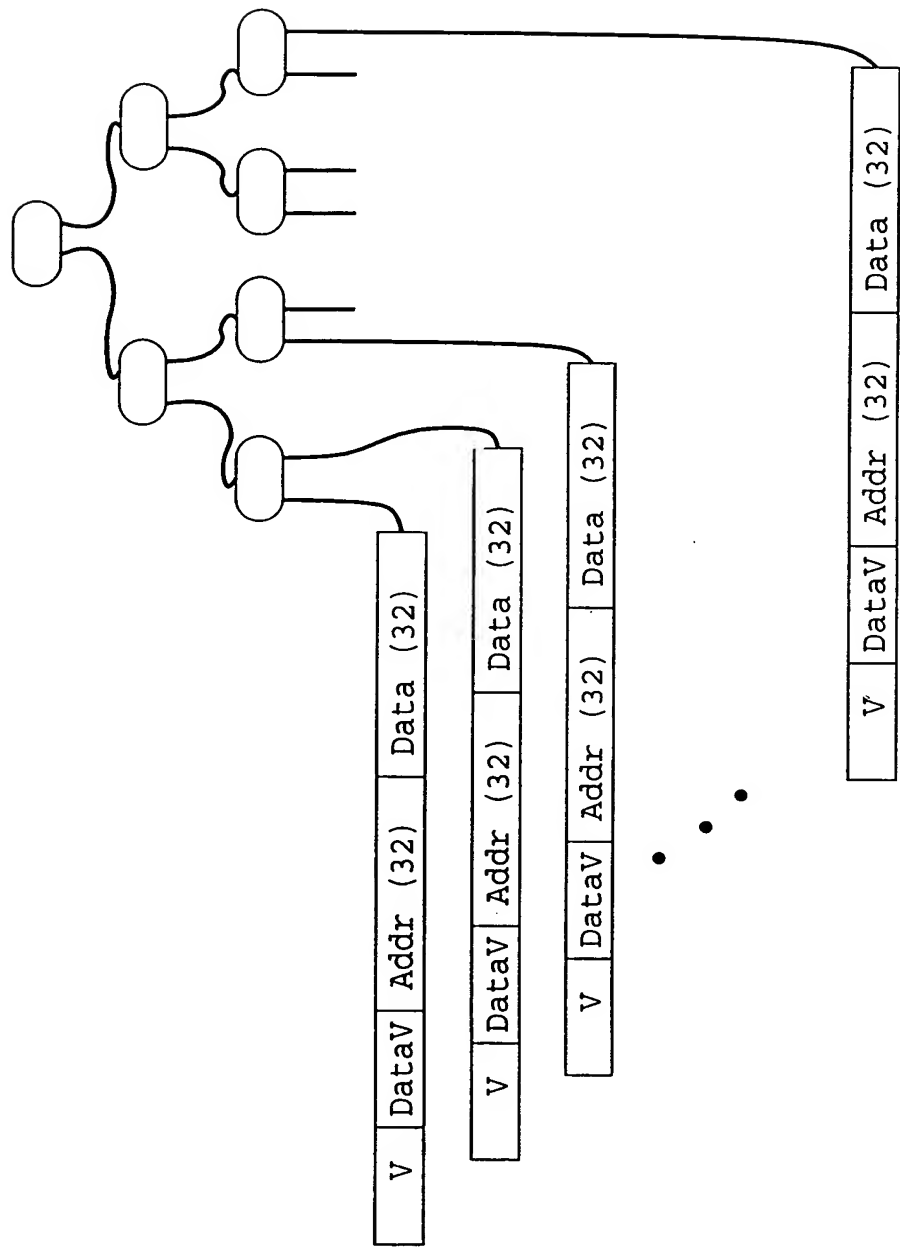


FIG. 36

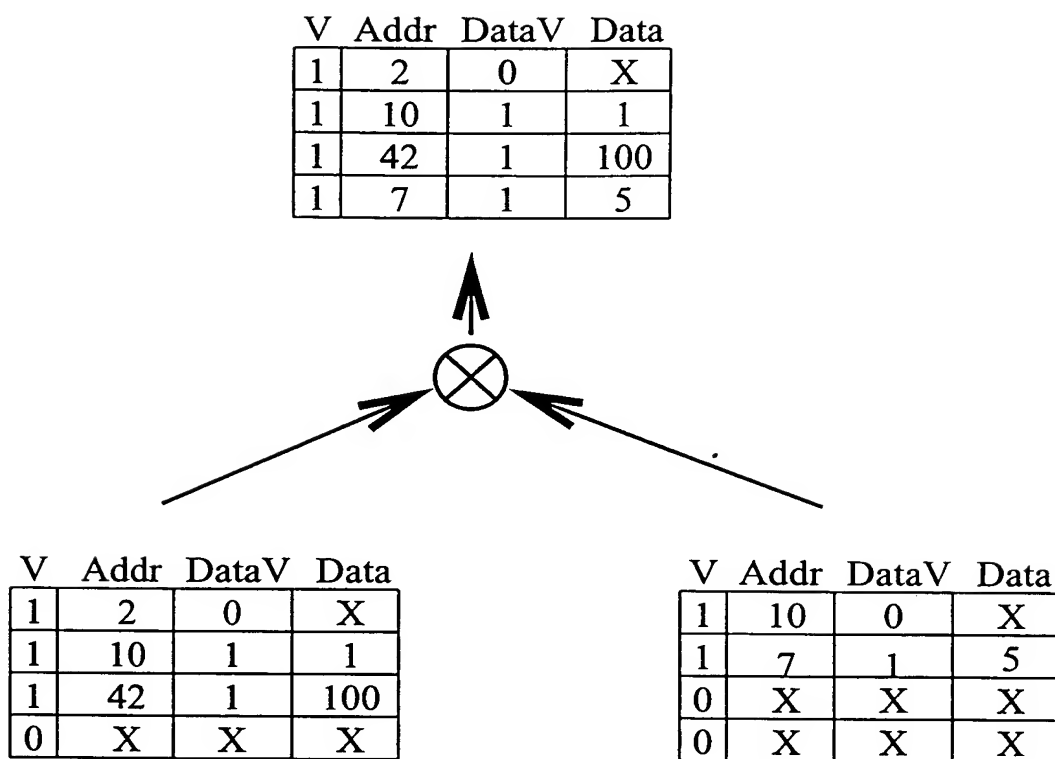


FIG. 37

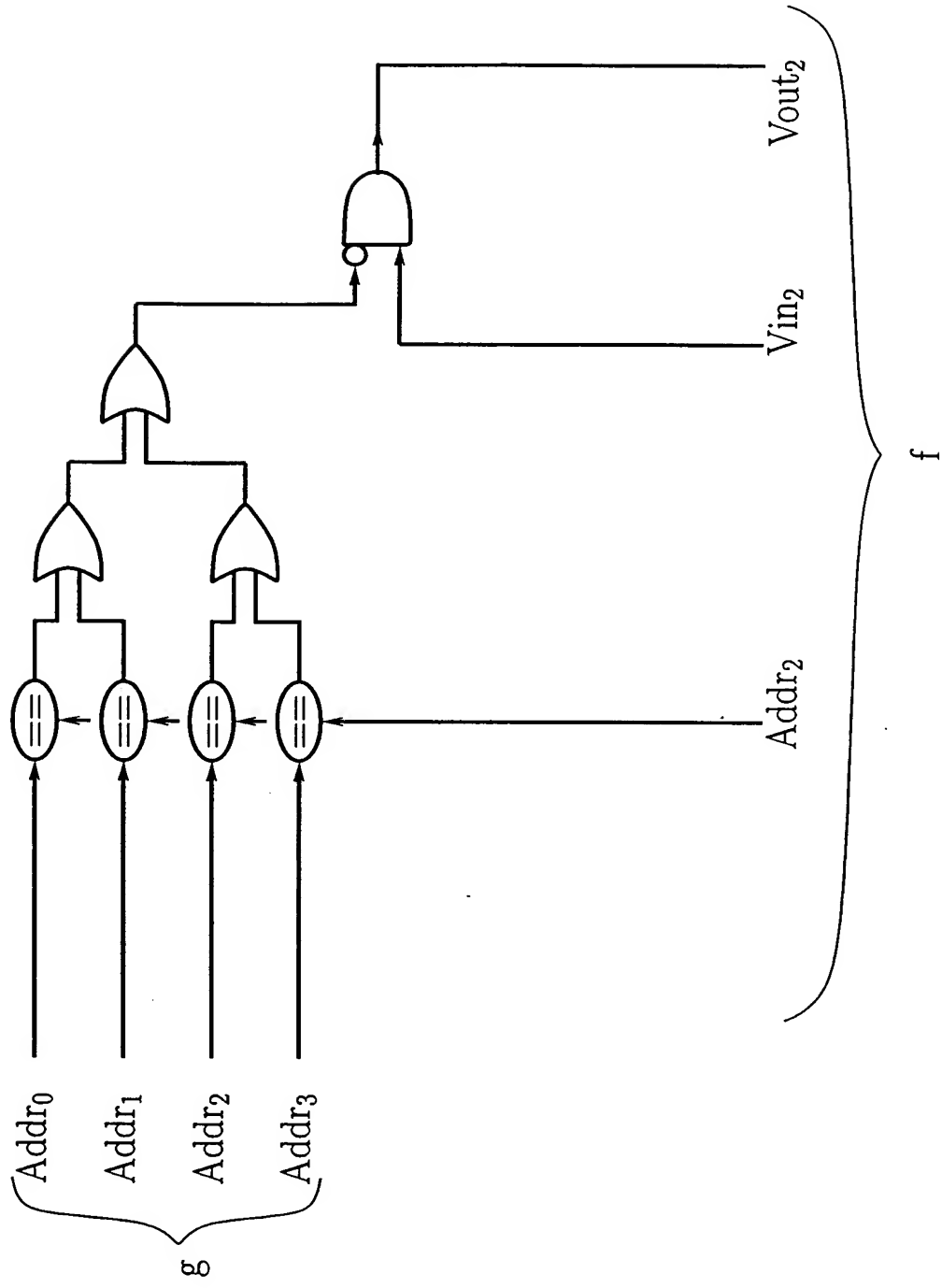


FIG. 38

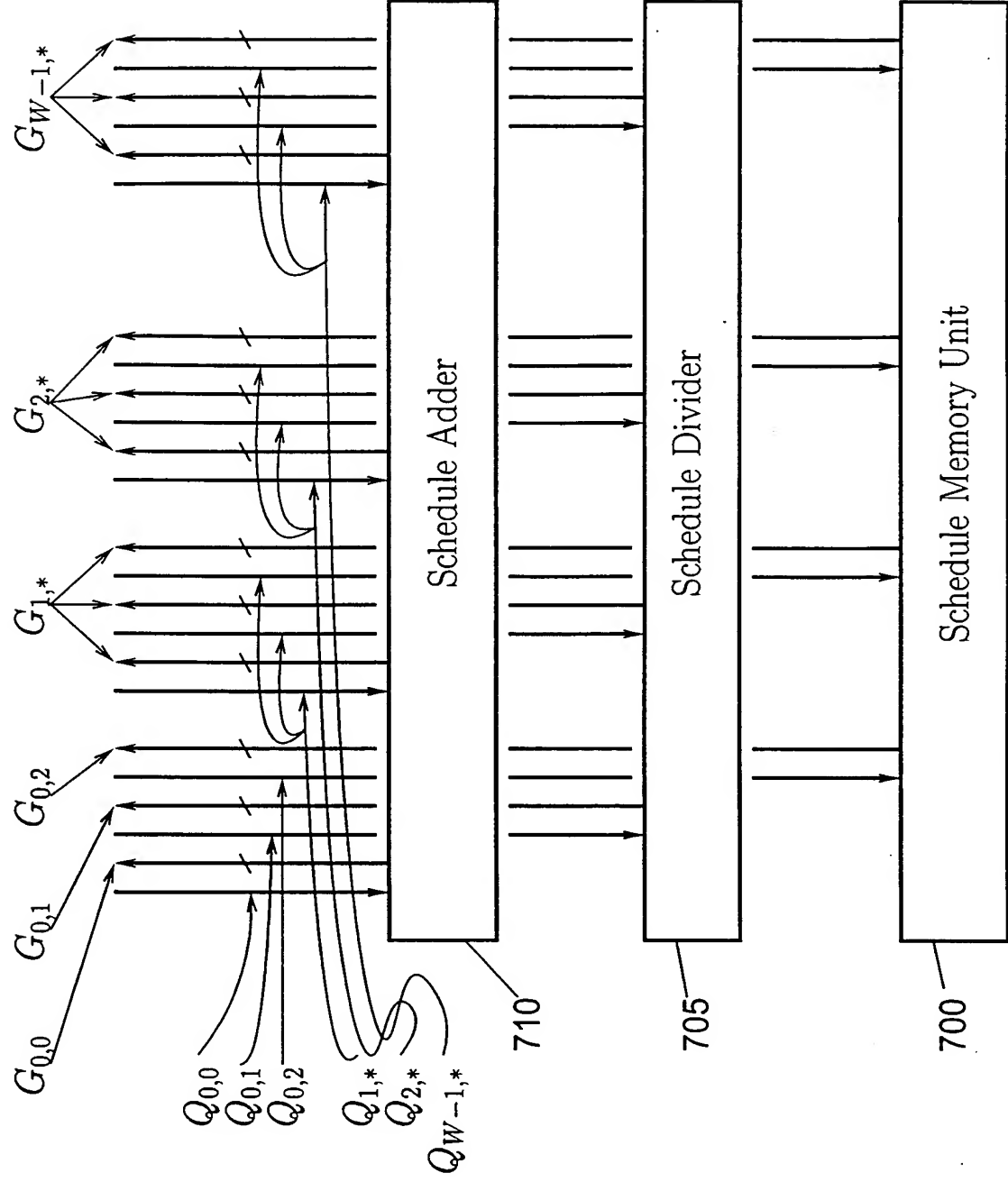


FIG. 39

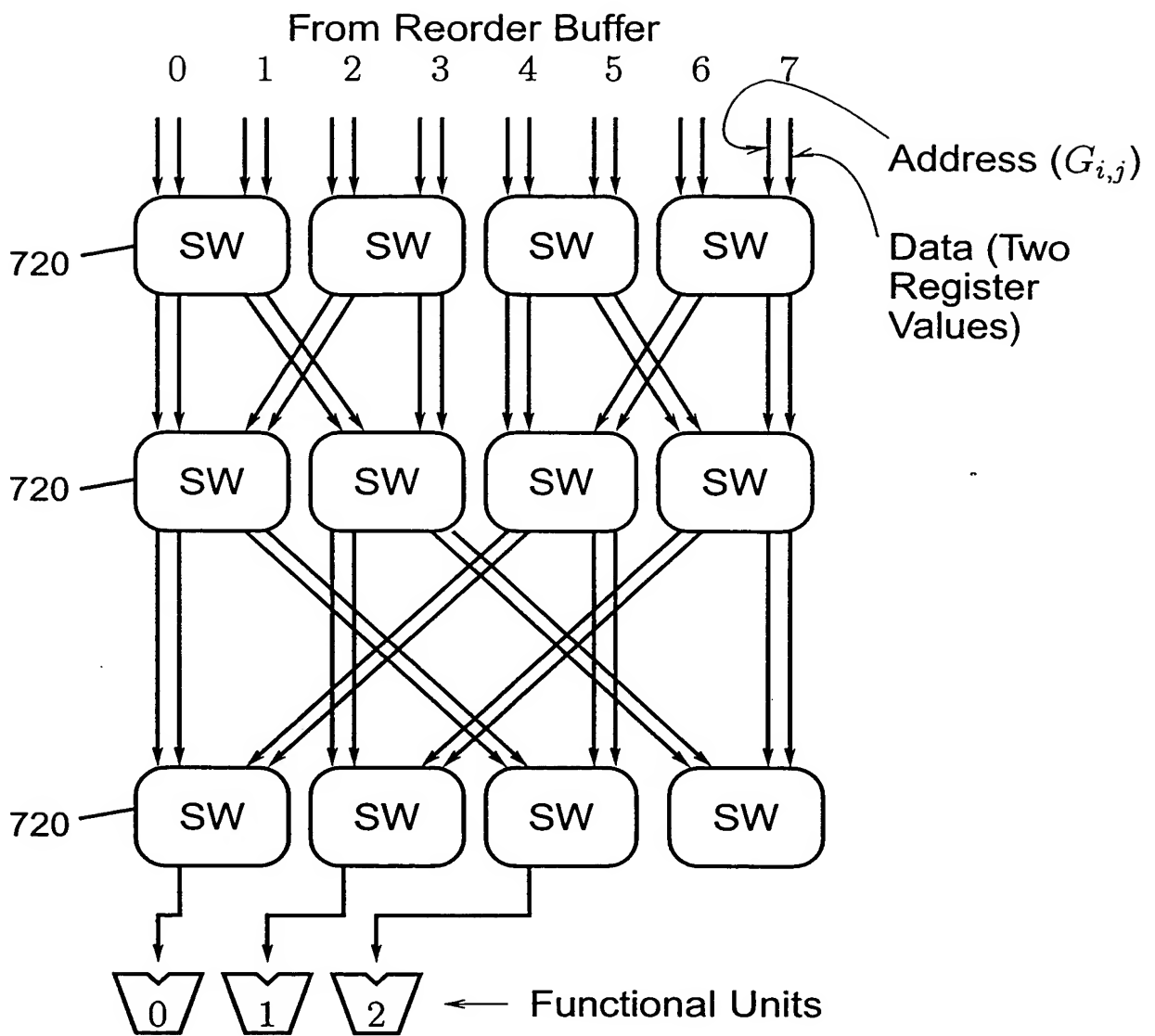


FIG. 40

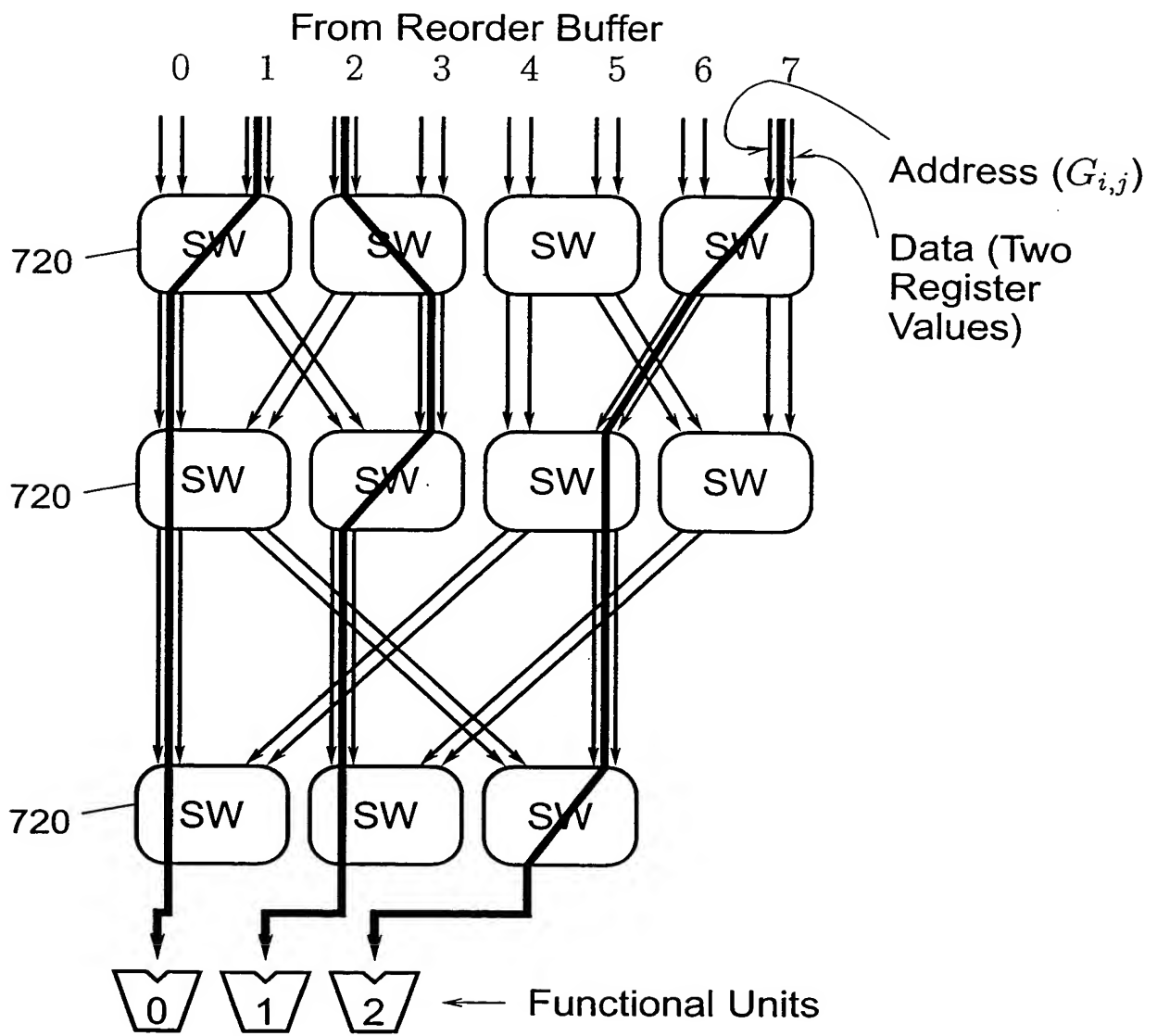


FIG. 41

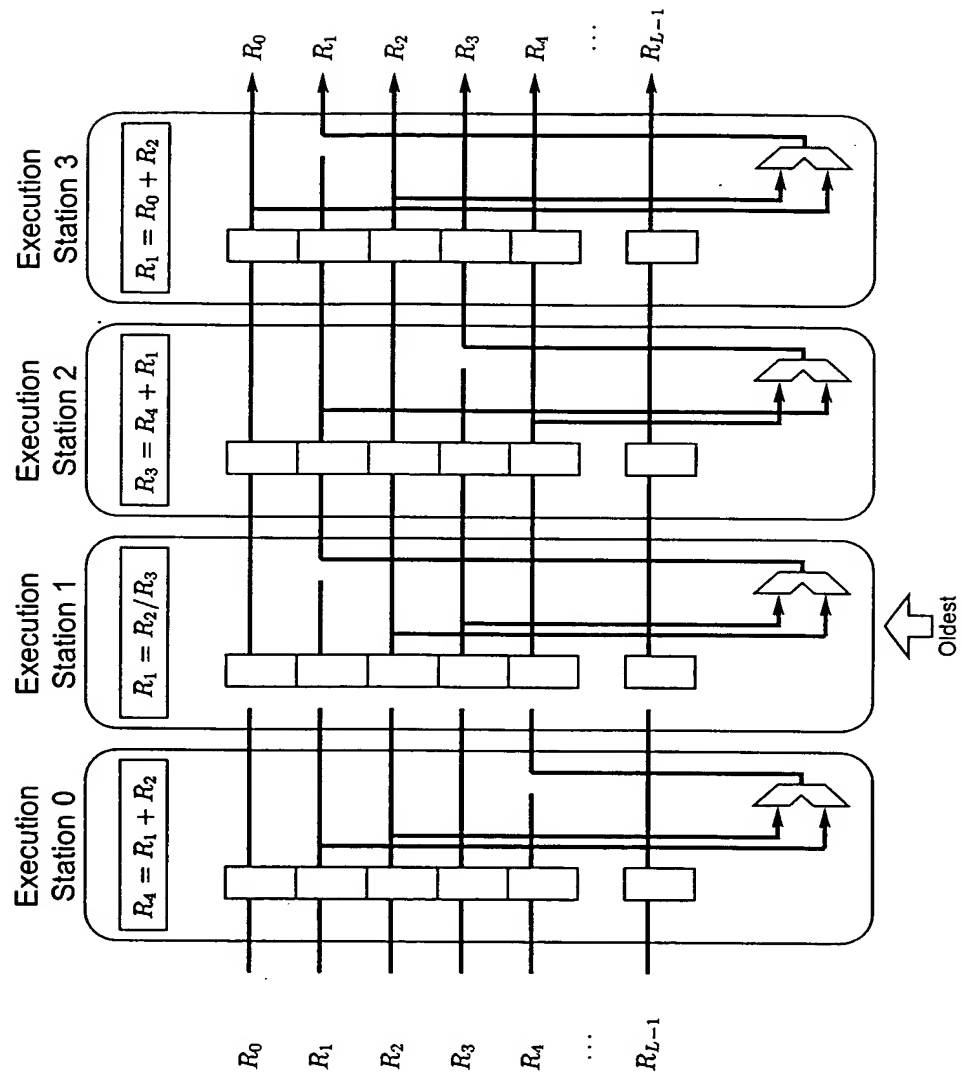


FIG. 42

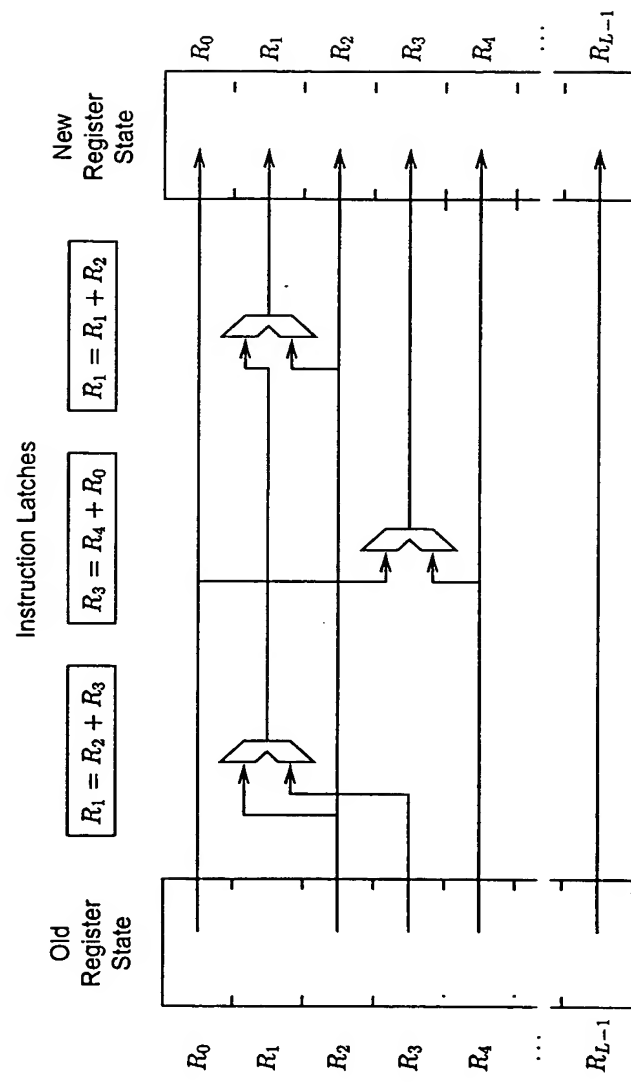


FIG. 43

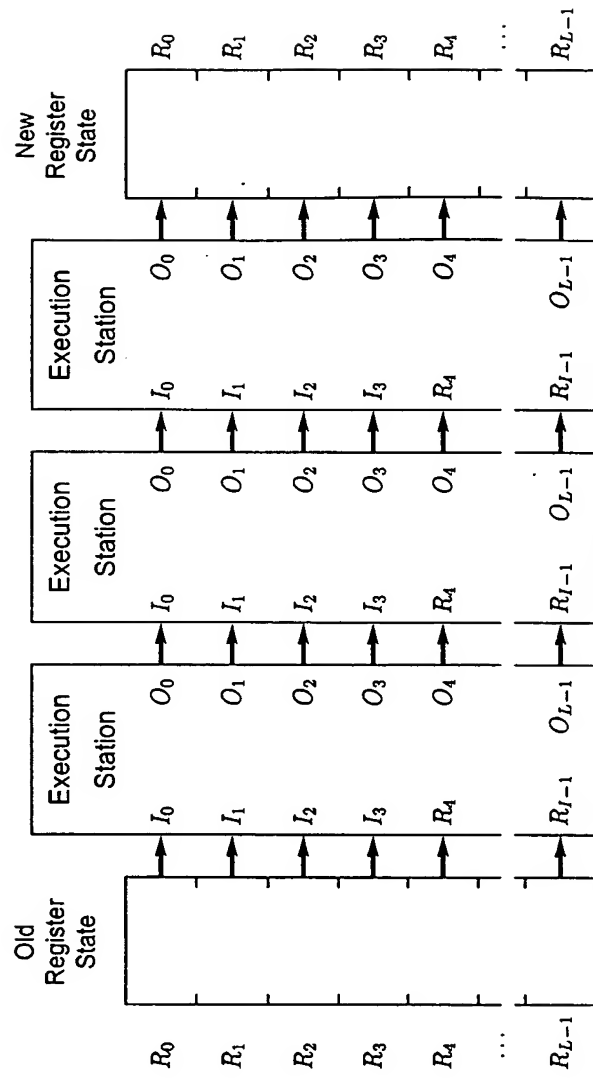


FIG. 44

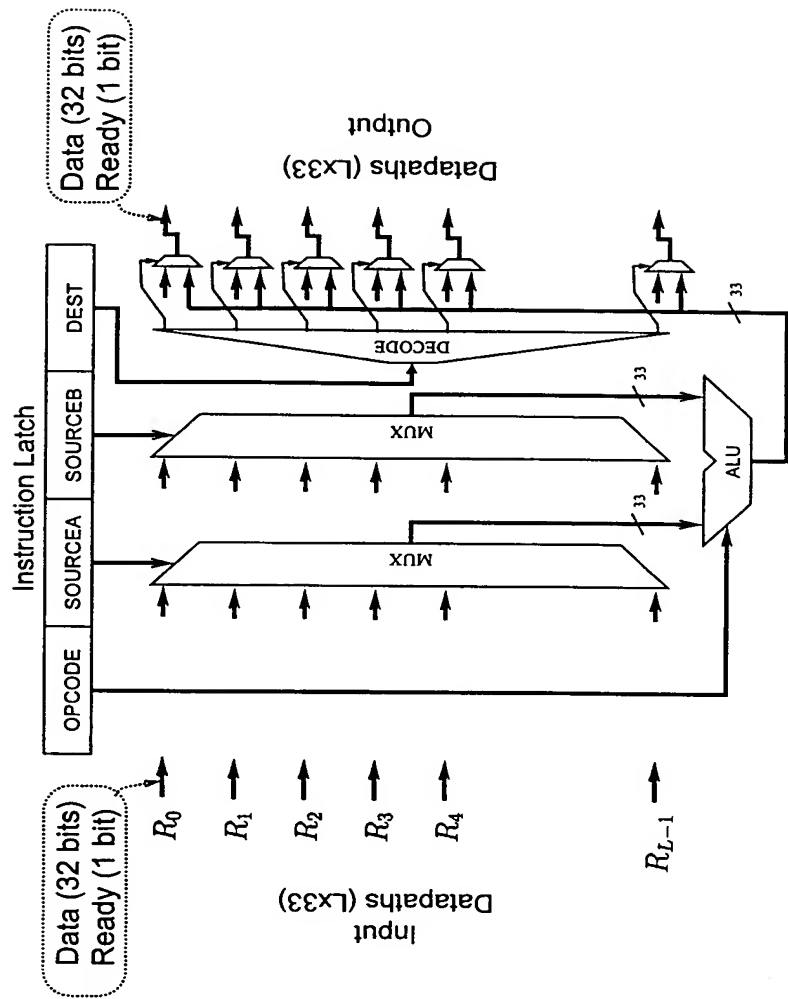


FIG. 45

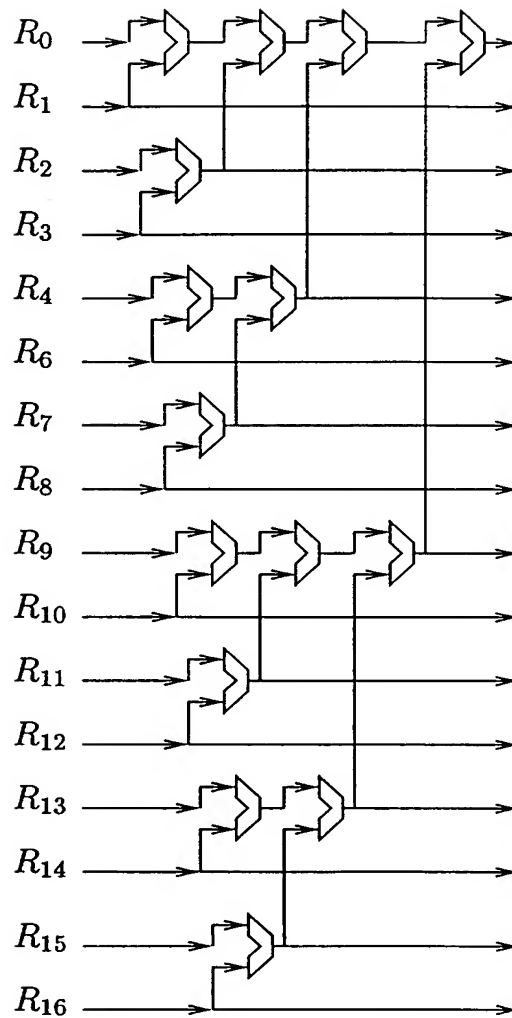


FIG. 46

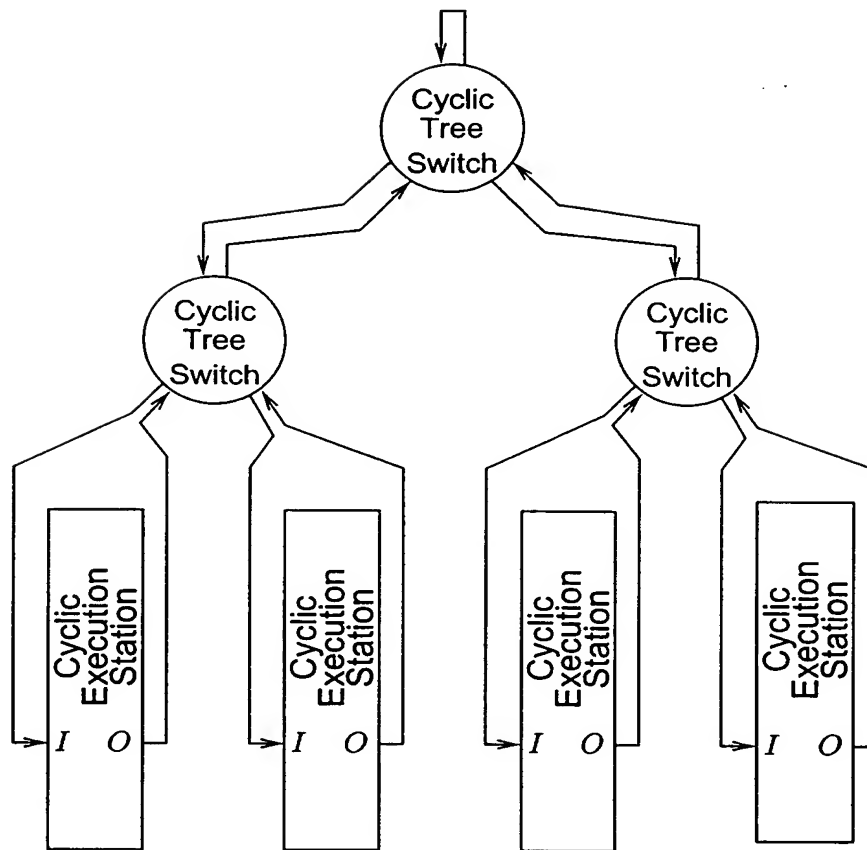


FIG. 47

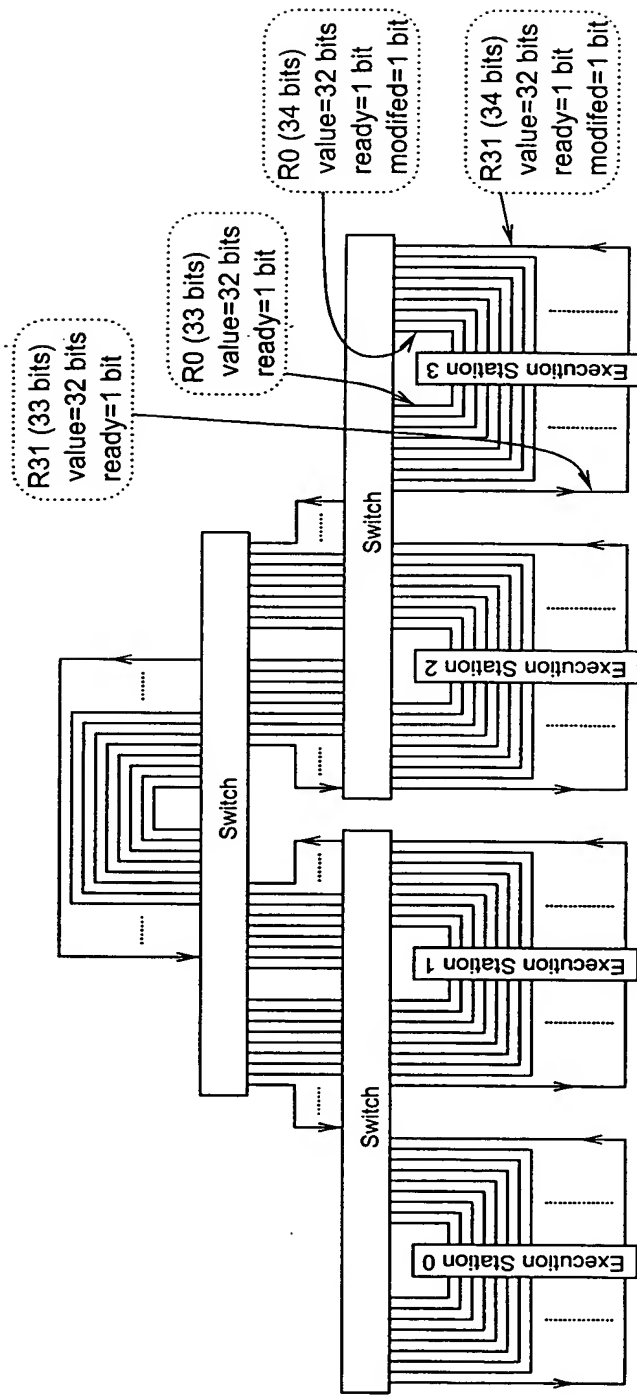


FIG. 48

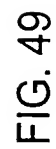


FIG. 49

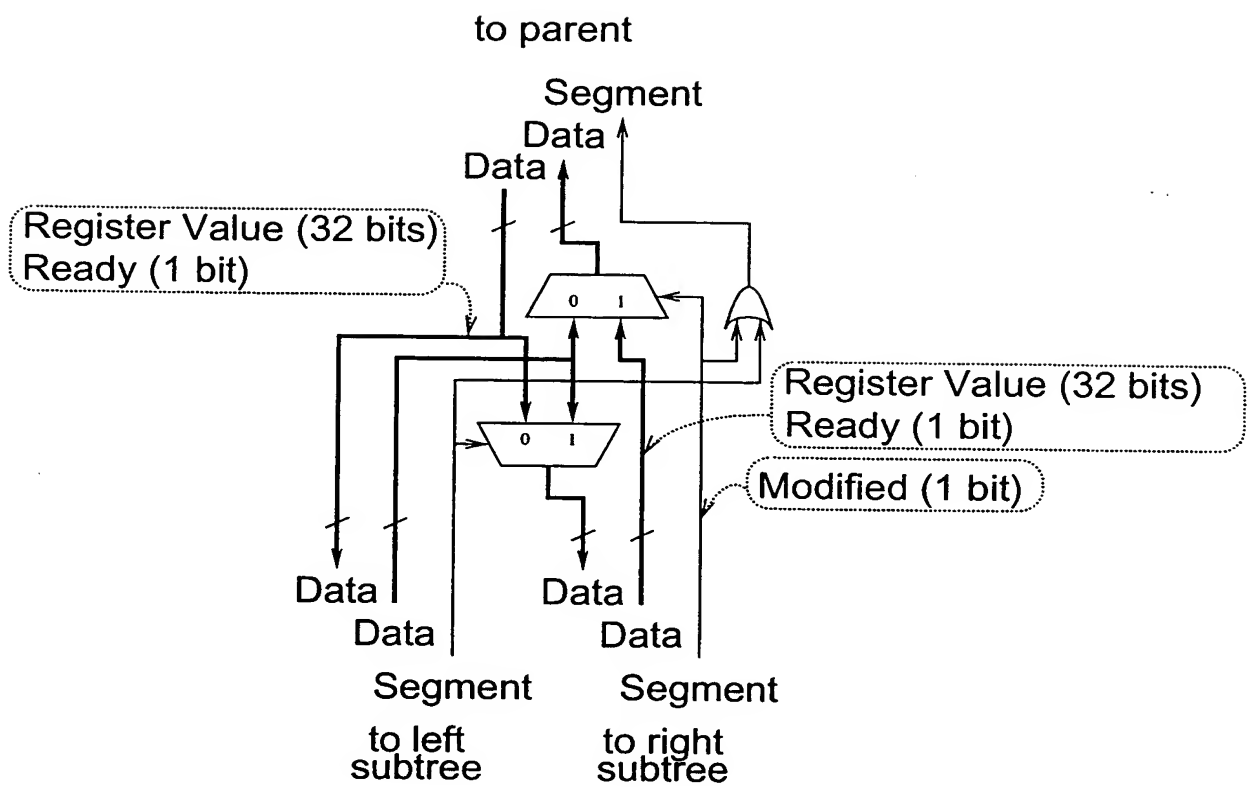


FIG. 50

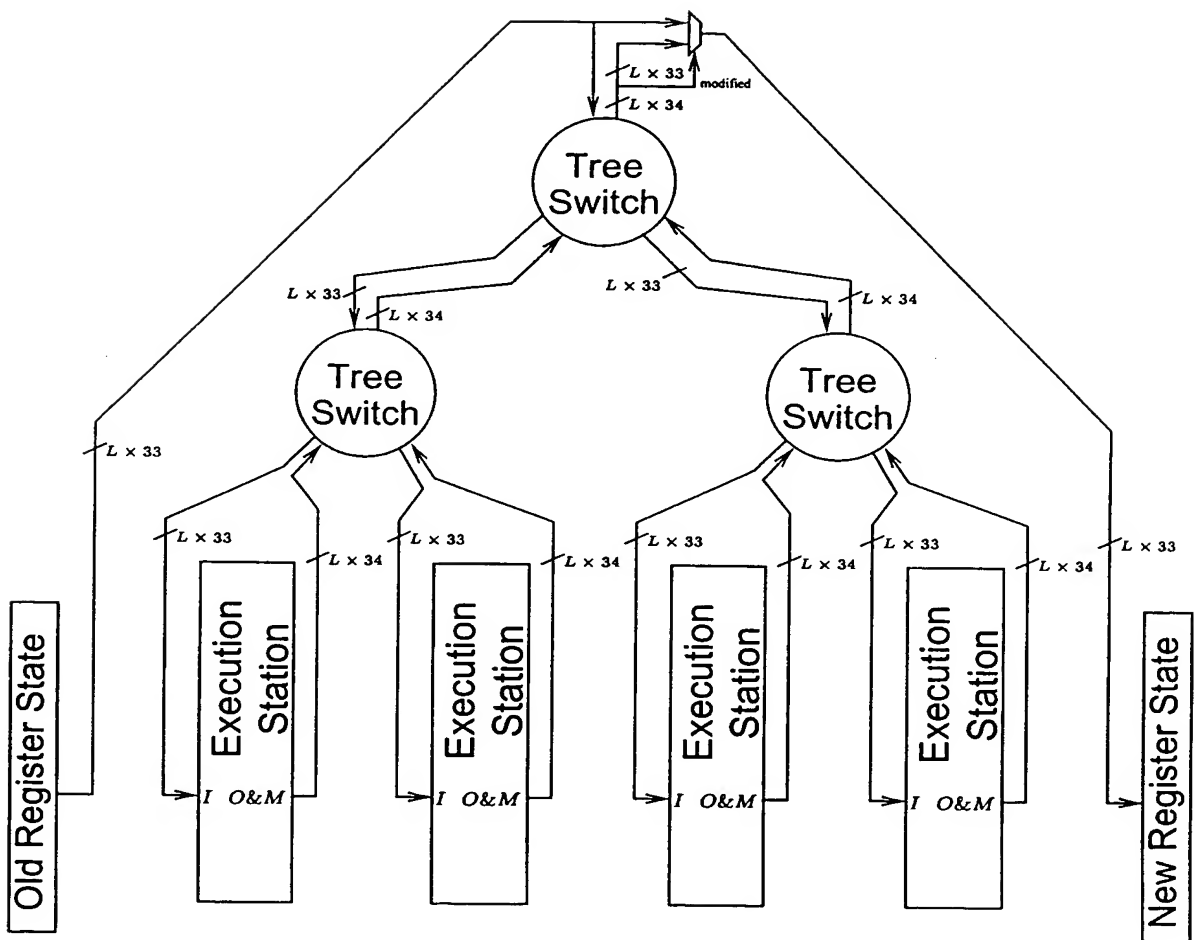


FIG. 51

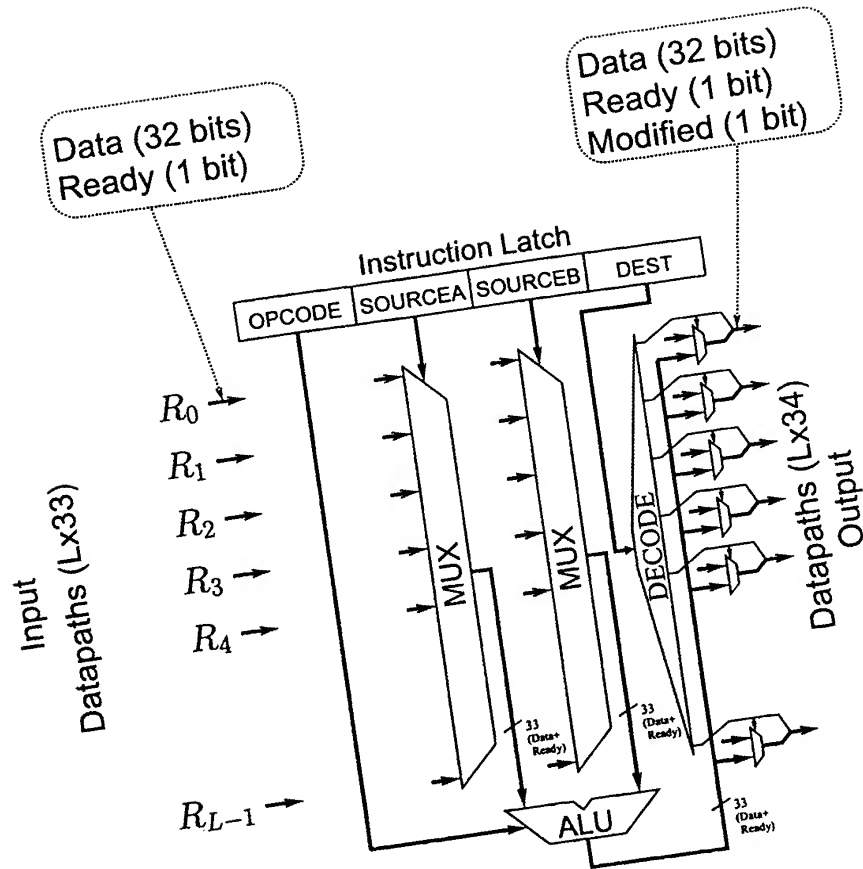


FIG. 52

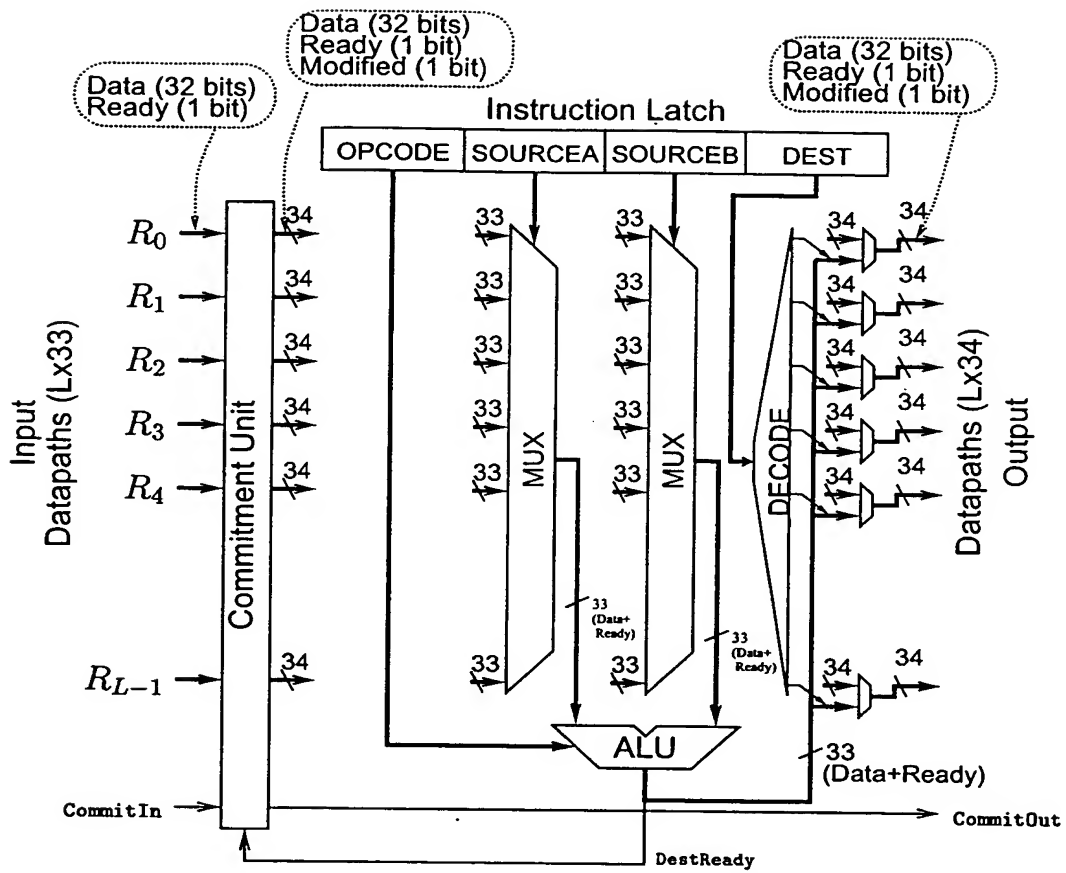


FIG. 53

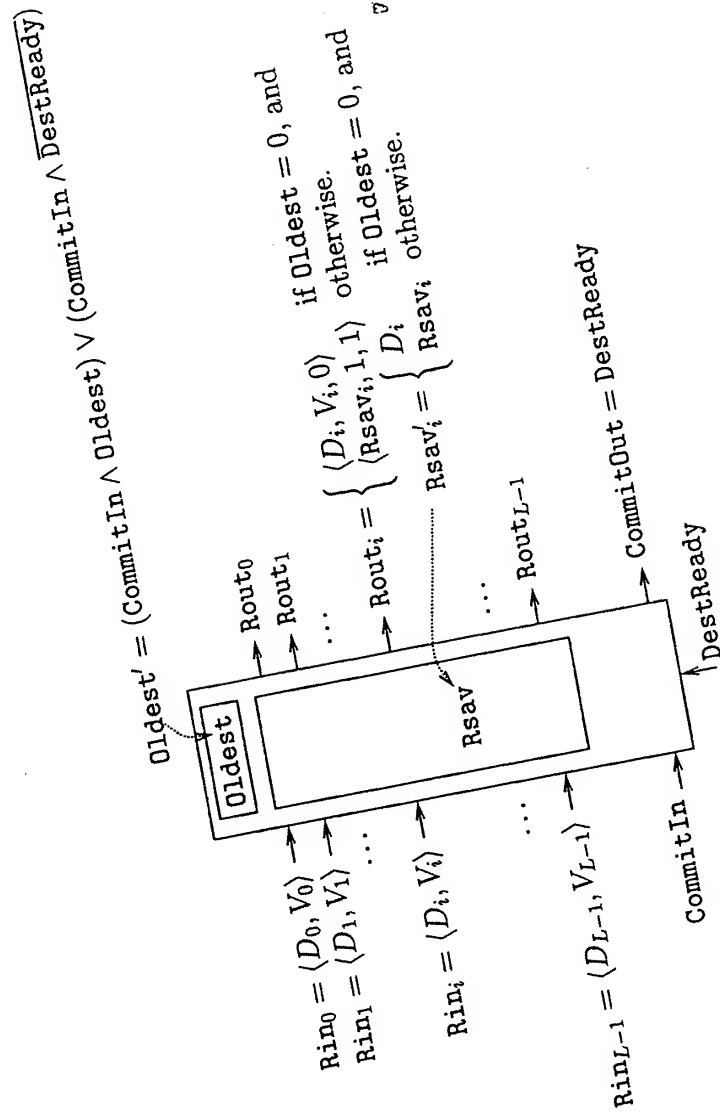


FIG. 54

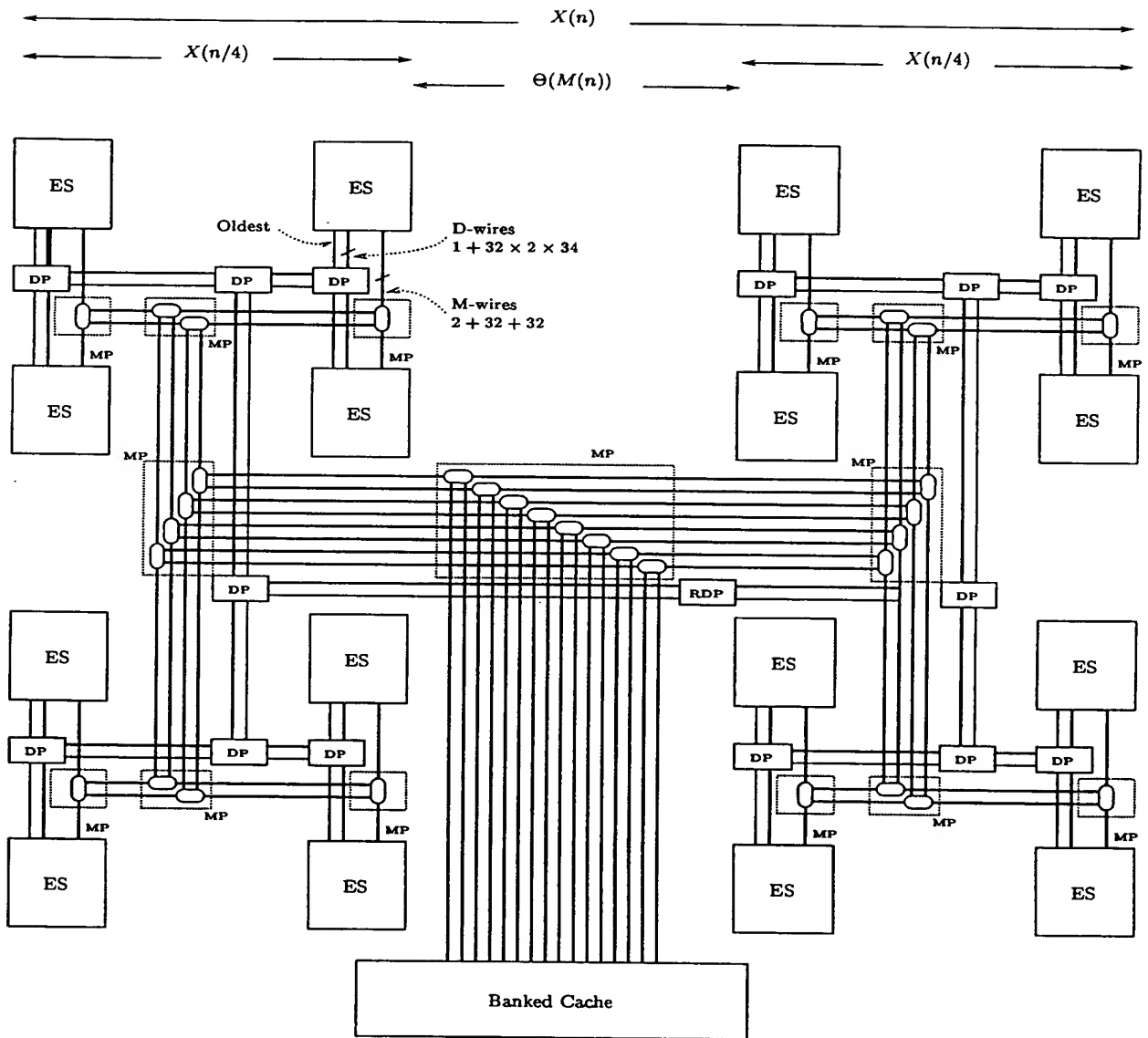


FIG. 55

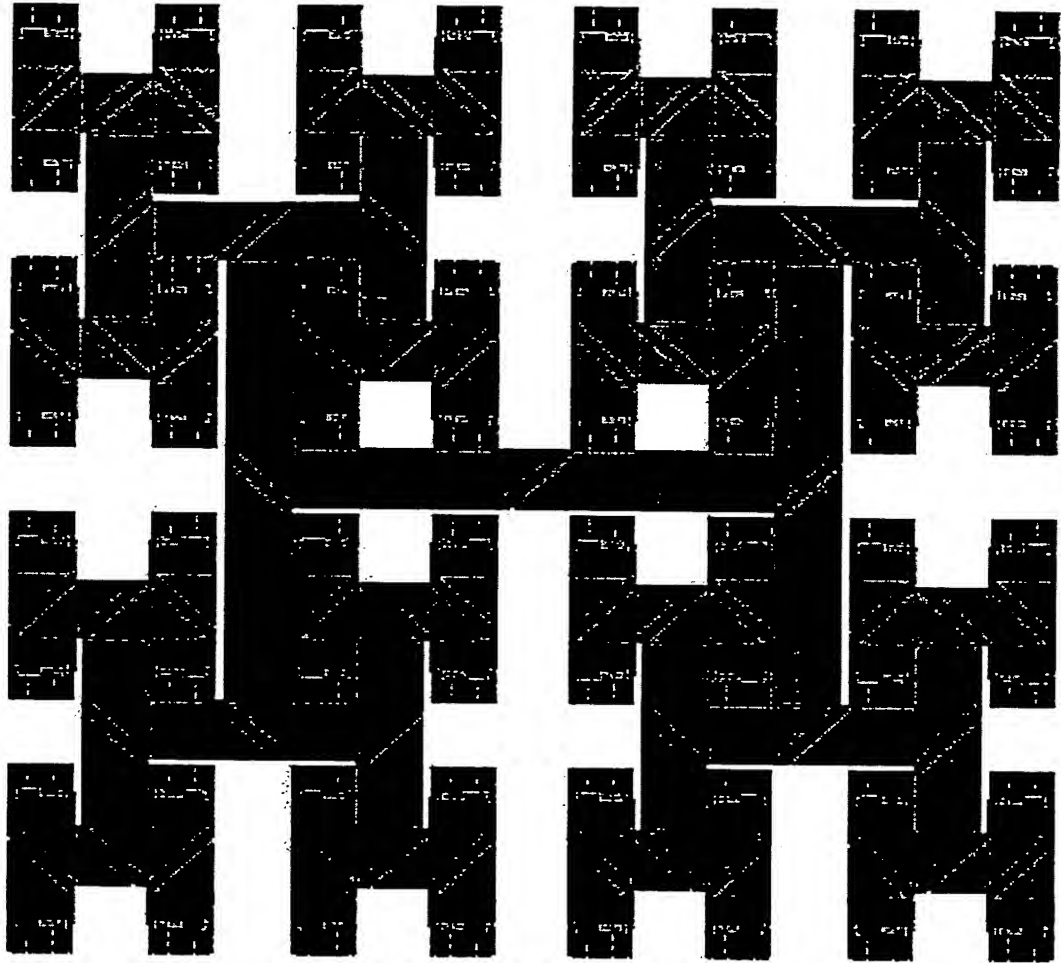


FIG. 56VLSI layout.

Committed Register File:

r1=0
r2=0

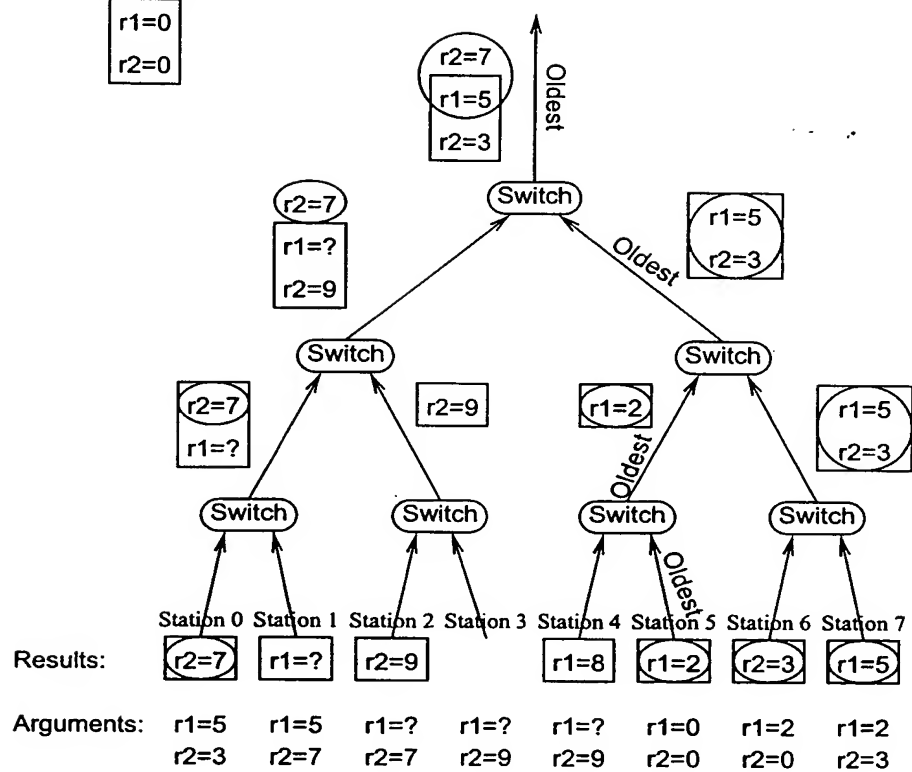


FIG. 57

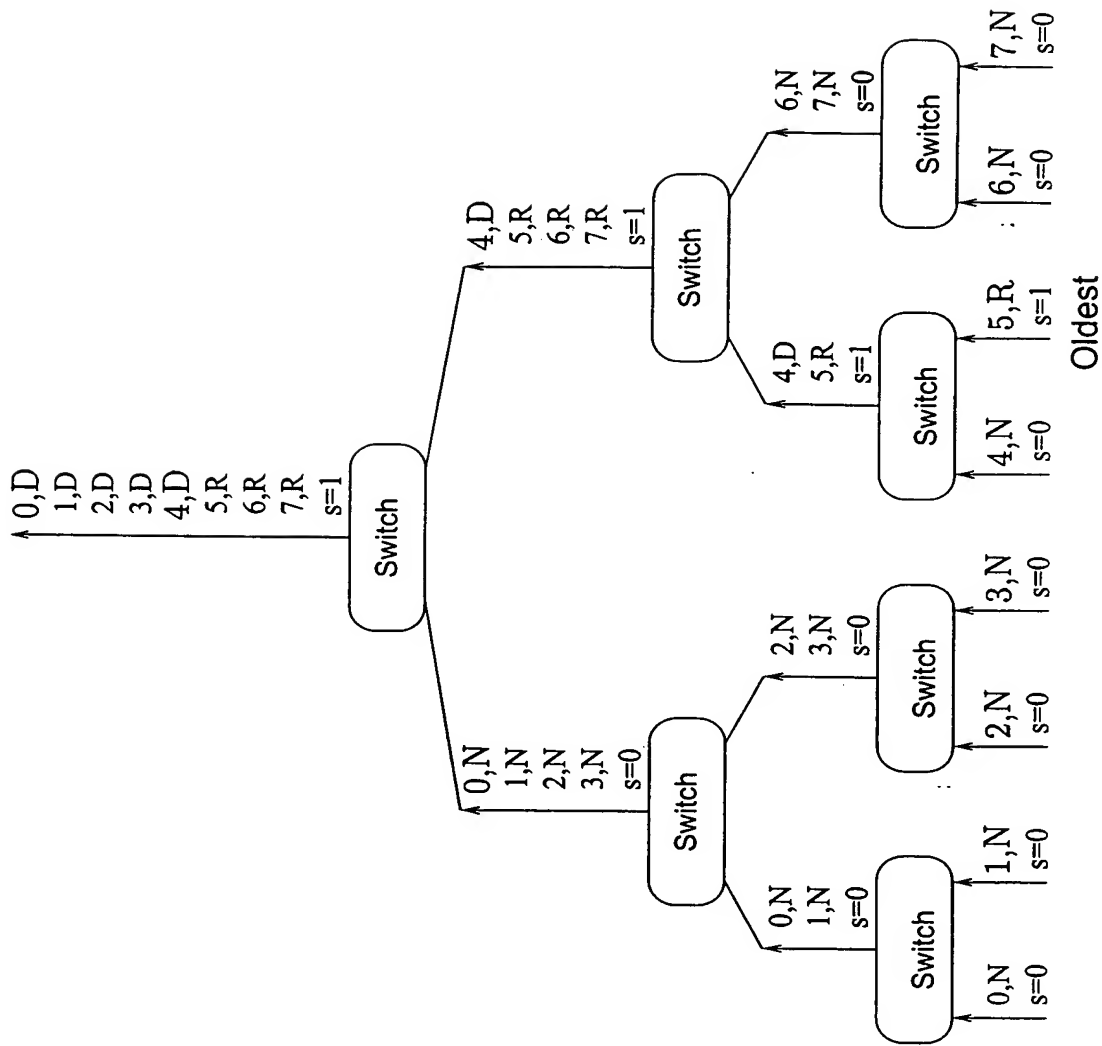


FIG. 58

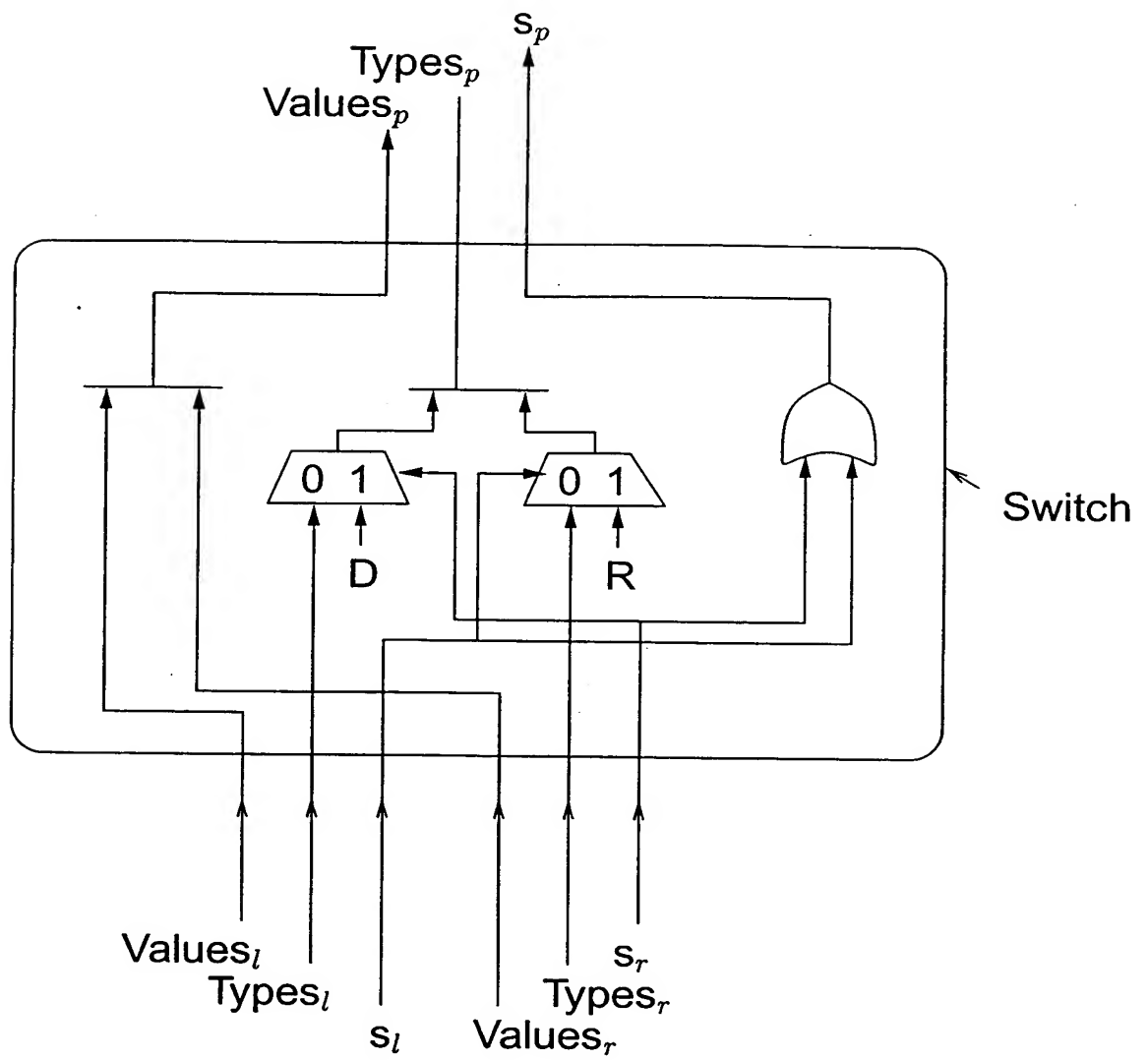


FIG. 59

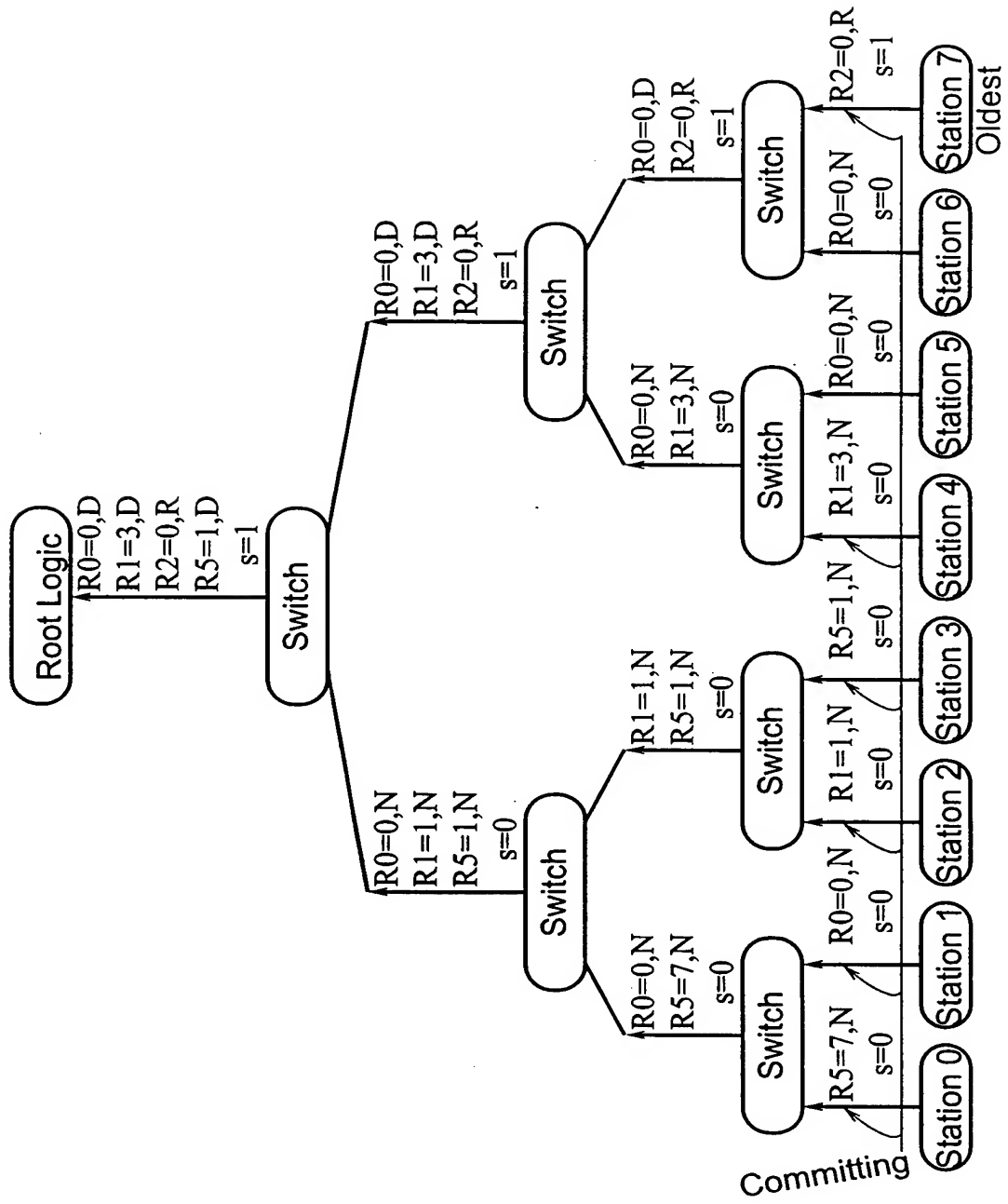


FIG. 60

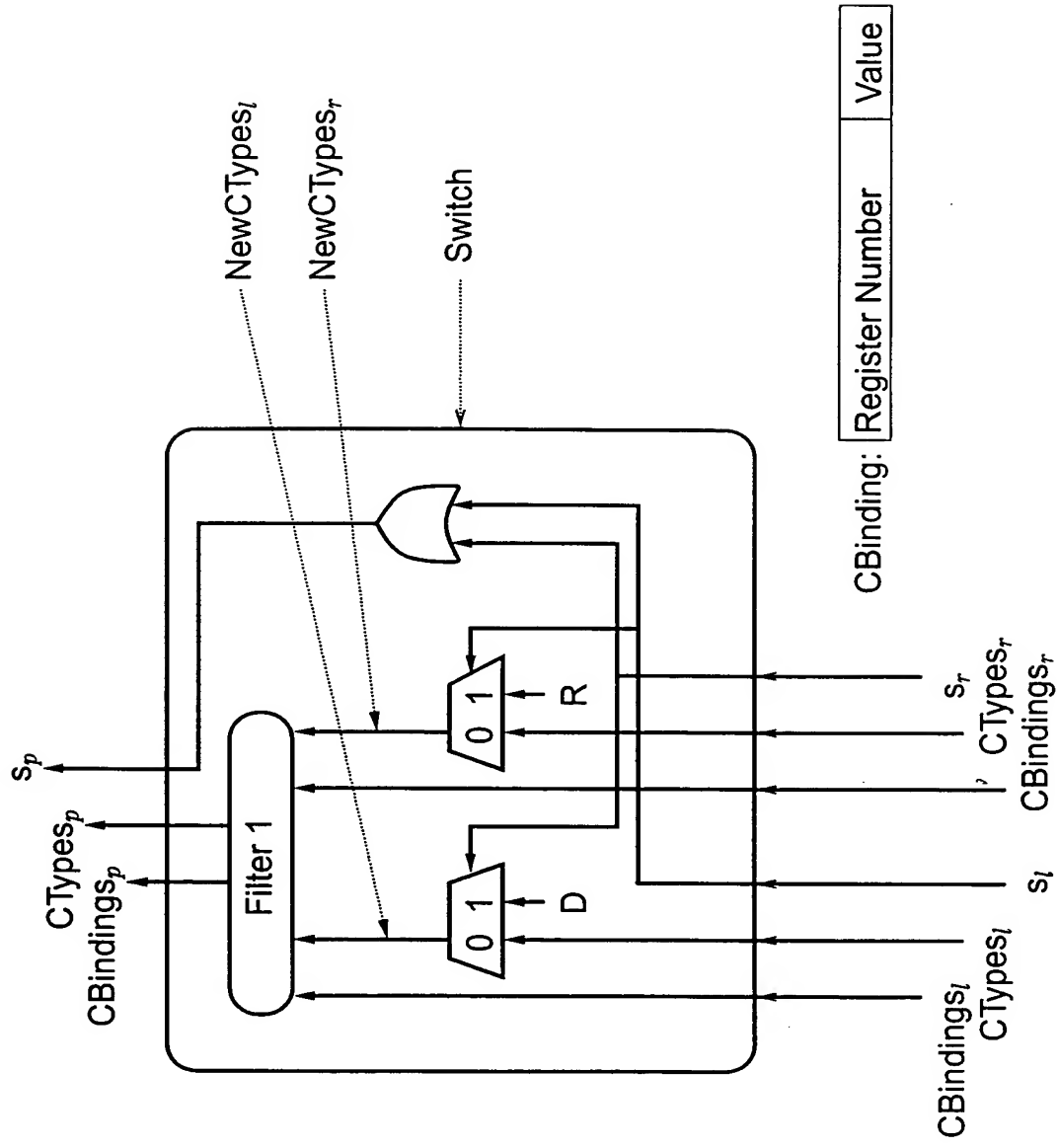


FIG. 61

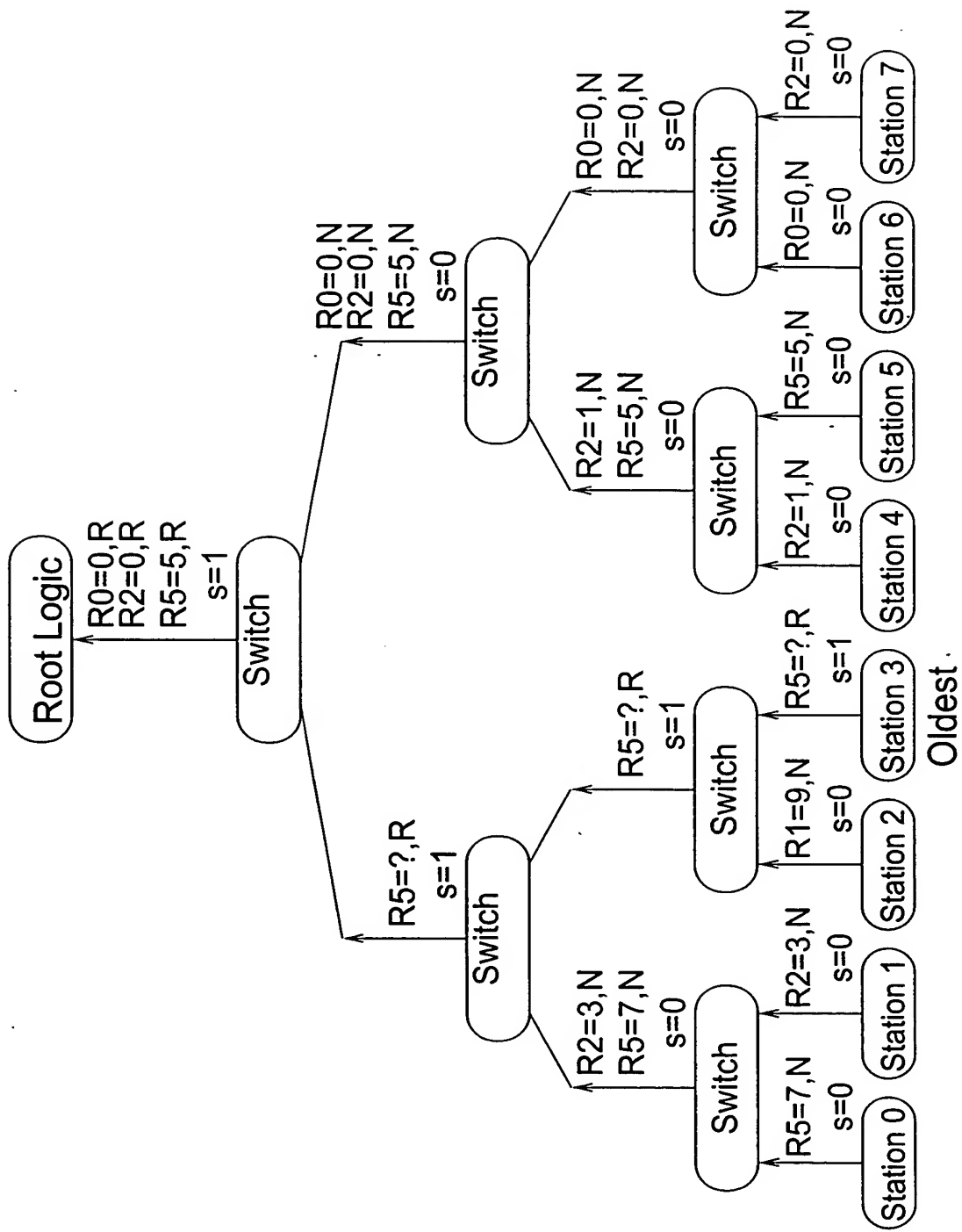


FIG. 62

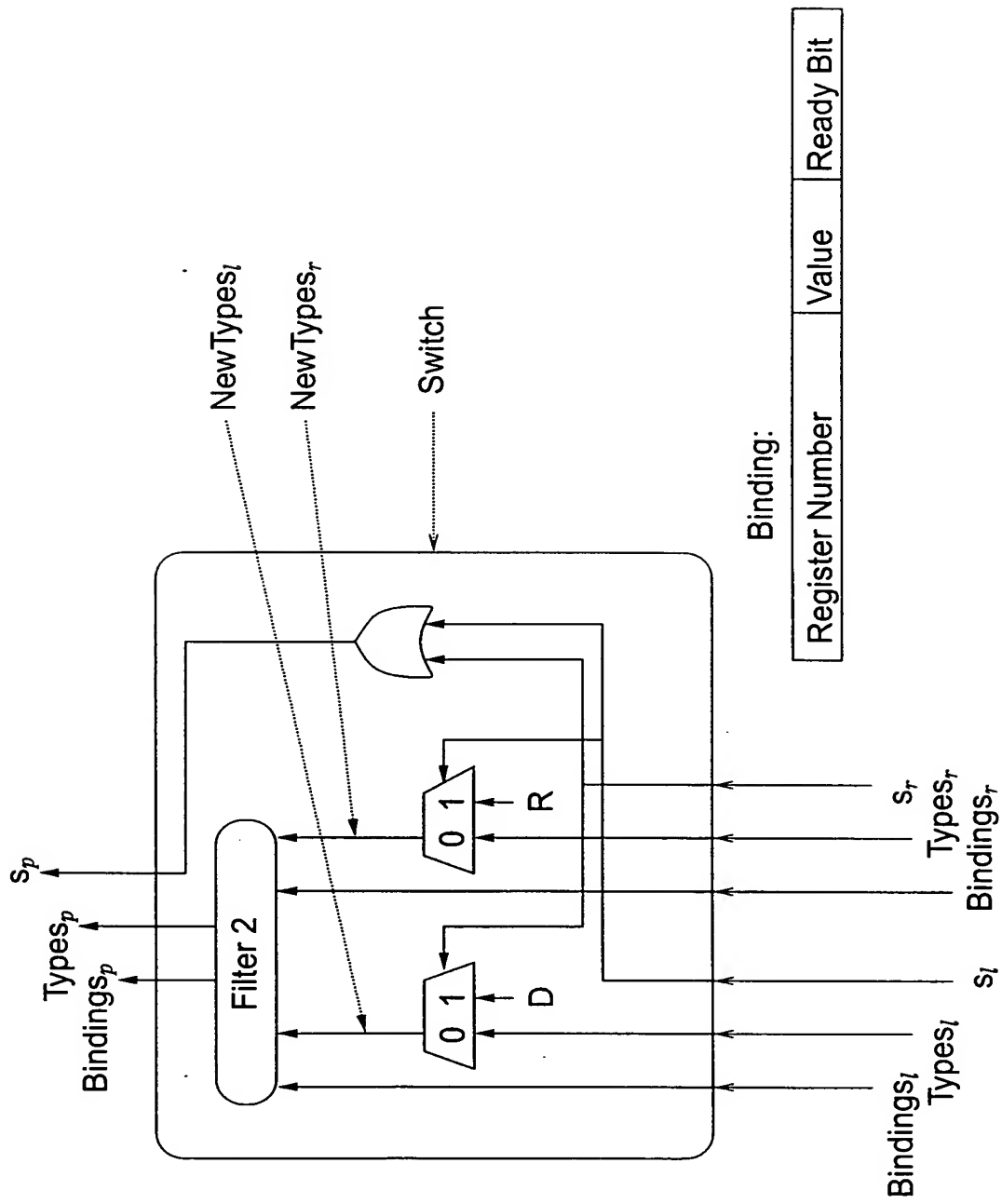


FIG. 63

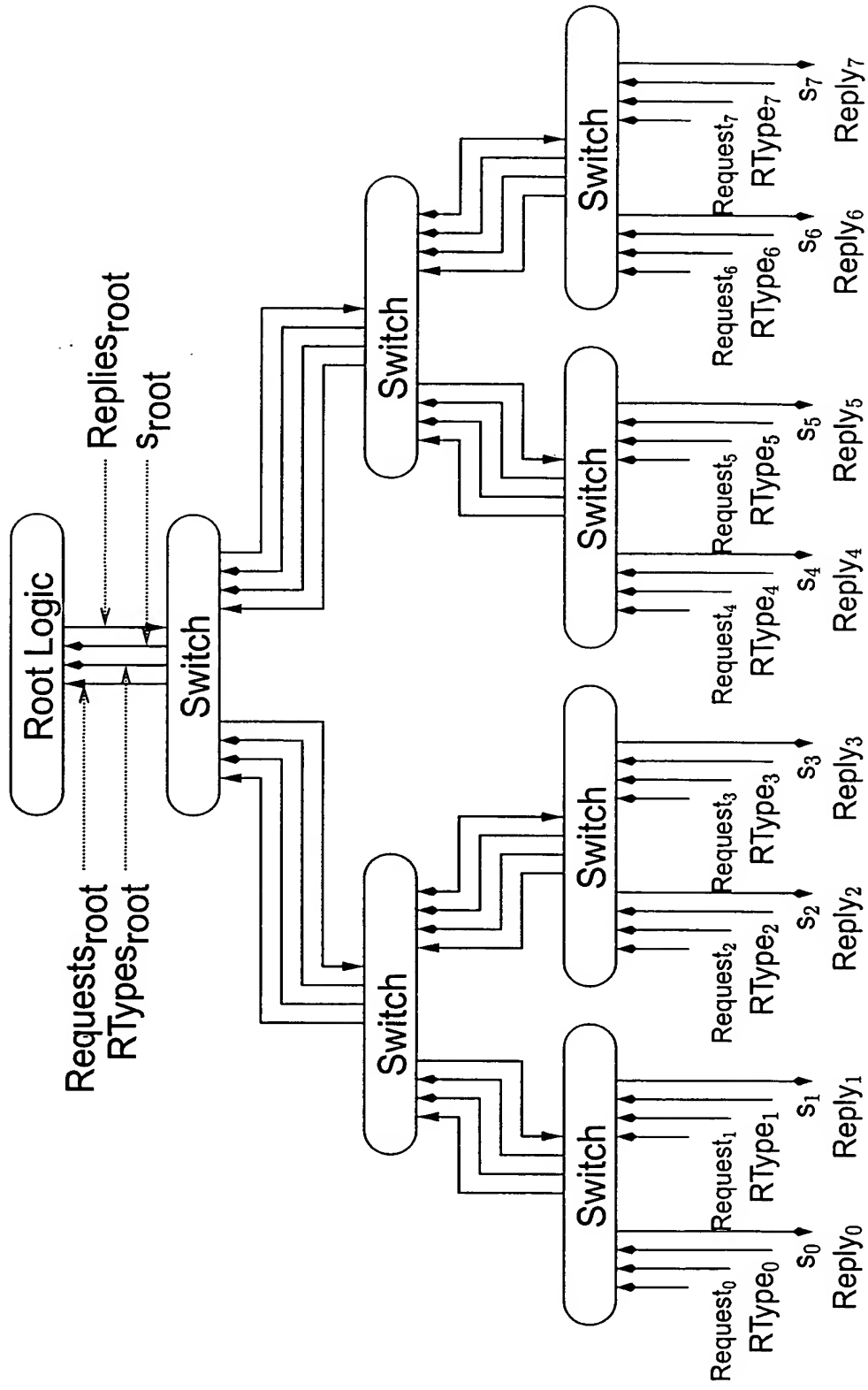


FIG. 64

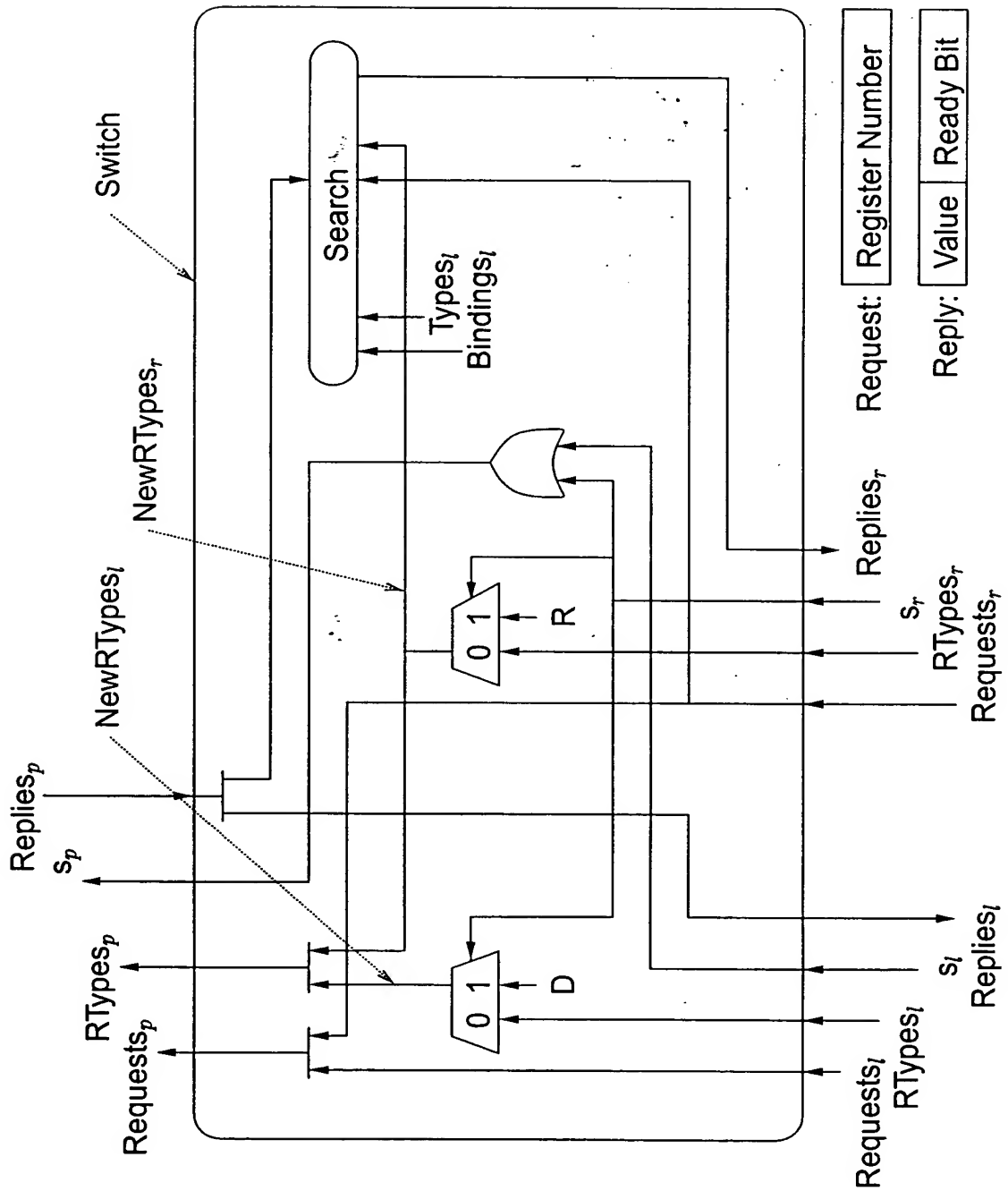


FIG. 65